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Light emitting field effect transistor with two self-aligned Si nanocrystal layers

V. Beyer,[1,a)] B. Schmidt,[1] K.-H. Heinig,[1] and K.-H. Stegemann[2]
[1]*Forschungszentrum Dresden-Rossendorf, Institute of Ion Beam Physics and Materials Research, P.O. Box 51 01 19, D-01314 Dresden, Germany*
[2]*Signet Solar GmbH, Am Fuchsloch 10, D-04720 Mochau, Germany*

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Light emitting field effect transistors based on narrow layers of silicon nanocrystals (NCs) in the gate oxide were fabricated. Direct quantum mechanical electron and hole tunneling into NCs was achieved by self-alignment of NCs-interface-distances to ~2 nm. The direct tunneling reduces oxide degradation, prolongs device lifetime and increases operation speed. Self-alignment occurs during thermal treatment of ion irradiated stacks of 50 nm polycrystalline silicon/15 nm SiO_2/(001)Si substrate. An alternating voltage (ac) was applied to the gate to inject charges into the NCs. Due to injection by direct tunneling, electroluminescence extends to higher ac frequencies than reported so far. © *2009 American Institute of Physics*. [doi:10.1063/1.3242379]

Ion beam synthesis (IBS) of nanocrystals (NCs) is compatible with modern complementary metal oxide semiconductor (CMOS) technology as it is a combination of ion implantation and subsequent annealing. Great effort is currently devoted to the IBS of semiconducting or metallic NCs for micro- and optoelectronic applications, respectively. An example is the nonvolatile multinanodot floating-gate memory.[1–4] Recently, Walters *et al.*[5] demonstrated a field effect driven electroluminescence (EL) by excitonic emission from Si NCs which are embedded in a gate oxide. An alternating current (ac) voltage is applied at the gate electrode of a MOS transistor device in order to charge the Si NCs sequentially with electrons and holes. Thereby, both charge carriers are injected from the transistor channel via Fowler–Nordheim (FN) tunneling through the oxide barrier. The excitons formed in the Si NCs recombine radiatively; the emitted wavelength depends on the NC bandgap energy, i.e., the NC size.[6]

Here, using an innovative fabrication process, a light emitting field effect transistor (LEFET) is demonstrated with two self-aligned luminescent layers of Si NCs. Compared to conventional Si NC synthesis by Si^+ ion implantation into the gate oxide (see Refs. 1 and 5, for instance), we take advantage of a self-alignment process, i.e., the Si NCs are formed in SiO_2 at a well-controlled small distance of ~2 nm from the Si/SiO_2 interfaces. This allows charge carrier injection into the NCs by direct tunneling, which leads to lower operation voltage and longer device life time. Additionally, excitonic light emission comes from two Si NC layers at the gate poly-Si/SiO_2 and the channel Si/SiO_2 interfaces. Figures 1(a)–1(c) illustrate the fabrication process. Ion irradiation through a MOS-like poly-Si/SiO_2/Si substrate stack [Fig. 1(a)] causes an ion-irradiation-induced mixing of both SiO_2/Si interfaces. At the formerly sharp SiO_2/Si interfaces nonstoichiometric SiO_x ($x<2$) regions are formed [Fig. 1(b)]. Subsequent annealing restores the upper and lower SiO_2/Si interfaces by phase separation (of SiO_x into SiO_2 and Si) [Fig. 1(c)]. In the tails of the ion beam mixed profile NCs form due to slow diffusion to the distance interfaces.[7–9] The competition between interface restoration and nucleation self-aligns the NCs into narrow layers parallel to the Si/SiO_2 interfaces. The competition between interface restoration and nucleation aligns the NCs into narrow layers parallel to the SiO_2/Si interfaces.[7] In comparison to the device reported by Walters *et al.*,[5] here, the light emission efficiency is improved due the additional second Si NC layer charged with opposite polarity from the poly-Si gate [see Fig. 1(d)]. The self-alignment of the NC layers with the SiO_2/Si interfaces allows to control shorter (direct) tunneling distances between the NCs and the Si electrodes with the potential of faster devices operating at reduced voltages. The charge storage

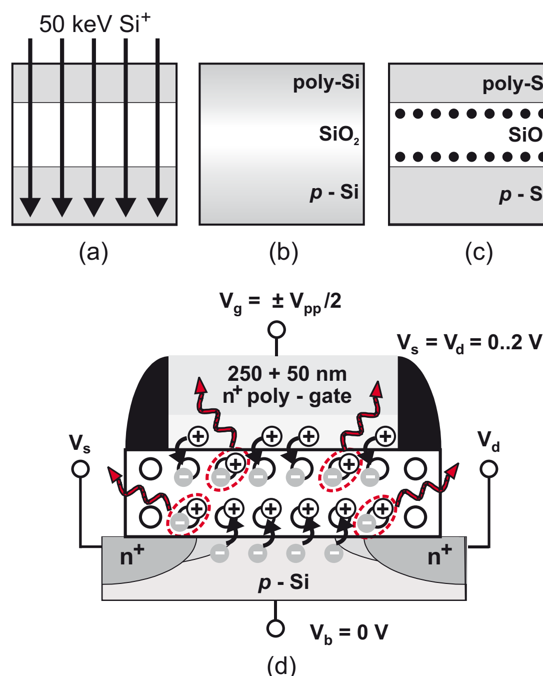

FIG. 1. (Color online) [(a)–(c)] Scheme of the fabrication of Si NCs in the gate oxide by ion irradiation through the Si/SiO_2 interfaces and subsequent annealing. (d) Schematic of light emission where an ac voltage is applied to the gate in order to inject charges of both polarities into the lower and upper Si NC layer from the channel and the poly-Si gate of the transistor, respectively.

a)Electronic mail: v.beyer@fzd.de.

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behavior of such a structure used as NCs based memory device is described elsewhere.[10,11]

In this article the performance of the LEFET devices as well as options of light emission with a NC double layer configuration are reported. A 14.5 nm thin SiO_2 layer was thermally grown at 900 °C for 50 min in dry O_2 on (001) *p*-type Si (1–10 Ω cm). A 50 nm thick poly-Si layer fabricated by low pressure chemical vapor deposition (LPCVD) covers this oxide. After 50 keV $^{28}Si^+$ ion irradiation of the poly-Si/SiO_2/*p*-Si layer stack to a fluence of 7×10^{15} cm^{-2} at room temperature [Fig. 1(a)], a highly n^+-doped 250 nm thick LPCVD poly-Si capping layer was deposited on top to form the poly-Si gate of the transistor. Rapid thermal annealing (RTA) was carried out at temperatures between 1000 and 1150 °C in N_2 for 10–160 s to prepare the Si NCs embedded in SiO_2 [see Fig. 1(c)]. The existence of the NCs was confirmed by EFTEM imaging using a FEI Tecnai 20 FEG microscope and a Gatan energy filter. Due to this protecting poly-Si layer the discussed fabrication approach profits by its insensitiveness to detrimental impacts.[4,8] The LEFETs were fabricated as *n*MOSFET devices with an active area of 20×20 μm^2 (gate length × gate width) using the standard 0.6 μm CMOS technology line of the Zentrum Mikroelektronik Dresden company. Originally prepared to study the memory characteristics of the embedded Si NCs, several layers of in total 3.2 μm thick Si_3N_4 and SiO_2 layers were deposited on top of the transistors. This device protection is usual in modern memory device fabrication but clearly not suitable for LEFET applications. Therefore, a second set of samples was prepared to study the photoluminescence (PL) properties of the embedded Si NCs, which was not possible on the integrated CMOS devices due to this multilayer coverage. For this sample series the preparation stopped after the 50 nm poly-Si layer deposition and subsequent ion irradiation. Here, the RTA treatment was carried out for 120 and 750 s and also for 3 h in a furnace, both at 1050 °C in N_2. Excited by the second-harmonics, 532 nm, of a Nd:YAG laser the PL spectra of the Si NCs were obtained by a liquid nitrogen cooled CD camera. ac square-wave voltage signals were applied to the gate with the *p*-Si substrate as the reference electrode and an amplitude between ±7 and ±11 V (peak-to-peak voltage V_{pp} of 14 to 22 V) by a 20 MHz NF1930 arbitrary function generator. The source and drain voltages were set to $V_s = V_d = 0$ V. The EL spectra were recorded using an Andor DU401A-UV-BR-DD CCD camera working at $T = -70$ °C (thermoelectrical cooling), a Shamrock 303i grating spectrometer, and an optical microscope.

TRIDYN ion collision cascade simulations reveal[7,12] that the 50 keV Si^+ ion irradiation of the LEFET layer stack causes an ion beam mixing of the poly-Si/SiO_2 and SiO_2/(001)Si interfaces with a considerable Si excess in the gate oxide. As the projected ion range is located deeply inside the Si substrate, the majority of Si excess results from ion beam mixing of the interfaces. As shown in Fig. 2 during annealing well-aligned narrow layers of Si NCs with 2–3 nm in diameter form adjacent to the recovered interfaces. The layers are separated to the poly-Si gate and *p*-Si substrate, respectively, by an oxide of about 2 nm thickness, i.e., within a direct tunneling distance for electrons and holes. In the middle of the gate oxide an about 5 nm thin SiO_2 layer is found sandwiched between the NC arrays. Applying an ac

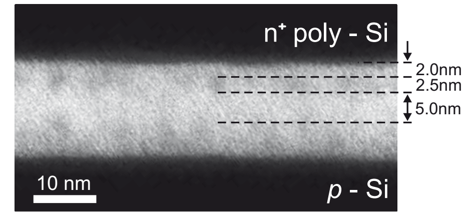

FIG. 2. Cross section EFTEM image of the poly-Si/SiO_2/*p*-Si layer stack revealing tiny Si NCs of about 2–3 nm size on both sides of the gate oxide in the late stage of ripening after 1100 °C, 160 s annealing.

voltage to the gate electrode—following the model of Walters *et al.*[5]—excitons are formed within the Si NCs due to alternating electron and hole injection from both electrodes. Since the emitted wavelength depends on the NC bandgap energy, i.e., the NC size, the luminescence with a center wavelength of about 750 nm as shown in Fig. 3 is attributed to radiative recombination of excitons within Si NCs of 2–3 nm in diameter which is consistent with the TEM result (Fig. 2).[5,6] The EL spectra in Figs. 3(a) and 3(c) were obtained from integrated devices of 20×20 μm^2 size. As confirmed by light transmission calculations (not shown here), the undulating modulations of the typically Gaussian-shaped luminescence profiles are related to multiple internal reflections within the Si_3N_4/SiO_2 multilayer stack covering the LEFET devices. These deviations are clearly not correlated with the NCs fabrication method since the PL spectra in Fig. 3(d), which are obtained at simple 50 nm poly-Si/14.5 nm SiO_2/Si stacks, reveal a typical behavior of tiny Si NCs. With the electro- and PL results in Fig. 3 different stages of NC evolution can be traced as a function of the annealing temperature and/or time. During the annealing at 1000 °C the overall EL intensity is close to its maximum value and

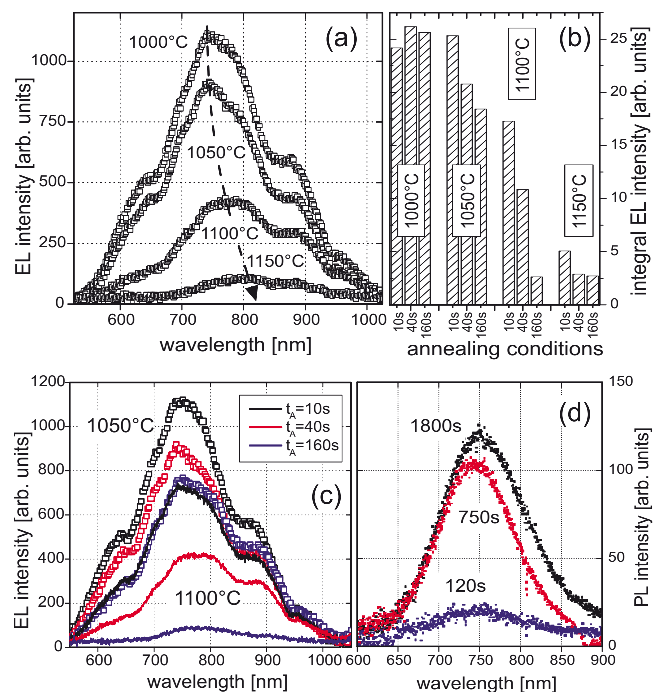

FIG. 3. (Color online) (a) EL spectra after 40 s annealing at different temperatures {$V_{pp} = 22$ V and $f = 10$ kHz in [(a)–(c)]}. (b) Bar graph plot of the integral EL intensities according to the total sample set (annealing for 10, 40, and 160 s at each temperature). (c) EL spectra after isothermal annealing at 1050 °C (squares) and 1100 °C (lines). The different annealing times are indicated by different colors. (d) PL spectra obtained at simplified structures after 120, 750 (RTA) and 1800 s (furnace) annealing at 1050 °C.

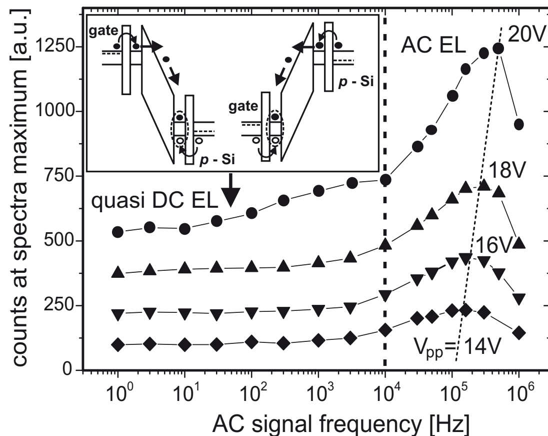

FIG. 4. Dependence of EL intensity on ac gate voltage amplitude and frequency for a LEFET annealed at 1050 °C for 40 s. A schematic band diagram illustrates the quasi DC mode EL mechanism in the inset ($f \lesssim 10$ kHz) for negative and positive ac square-wave gate voltage periods.

still slightly increasing [see the bar graph plot of Fig. 3(b)]. With a higher thermal budget (1050 °C) the intensity is decreasing especially during the 1100 °C annealing down to a very low but stable level such as for 1150 °C thermal treatment. Whereas an increasing intensity indicates that the process of precipitation and Si NC formation has not been finished up to this state (1000 °C), the dissolution of NCs is beginning at 1050 °C; the evolution of the NC size follows Gibbs-Thomson's relation, i.e., a diffusion controlled ripening process.[7,9] NCs adjacent to the Si substrate and poly-Si gate dissolve the faster, the closer they are located to the Si/SiO_2 interfaces.[7–9] This accelerates the dissolution of small, close NCs (1100 °C) and stabilizes bigger more distant ones (related to the Si substrate and gate, respectively) like for 1100 °C, 160 s and 1150 °C annealings in Fig. 3(b). During Ostwald ripening the Si NCs compete with each other in plane whereas some Si NCs grow at the expense of smaller ones. This corresponds at the same time to (i) the redshift of the EL spectra in Fig. 3(a), i.e., a radiative exciton recombination in larger NCs (which are characterized by a smaller bandgap), and (ii) the quenched luminescence due to a considerably reduced number of light emitting sites. It has to be mentioned that the denoted LEFET annealing temperatures represent only a part of the total thermal budget necessary for complete CMOS device fabrication. This explains why the overall PL intensity in Fig. 3(d) is still increasing during isothermal annealing indicating that the process of Si formation has not been finished after 1050 °C, 750 s, while seemingly the EL intensity already decreases with 1050 °C, 40 s thermal treatment [Fig. 3(c)].

The LEFET has two luminescence options depending on the applied gate signal frequency (Fig. 4). With similar EL spectra we refer both modes to radiative recombination of excitons in the Si NCs. At low frequencies, where both NC layers are saturated with charges of opposite sign, a quasi-direct current (dc) related EL is dominating (see the inset in Fig. 4). The applied gate voltage drops mainly across the remaining 5 nm thin SiO_2 layer sandwiched between the NC arrays. This enables a dc leakage current due to FN tunneling of electrons which recombine radiatively with stored holes at the NCs of the opposite side. The quasi-dc current can be easily suppressed increasing the gate oxide thickness to quench the tunneling probability (with positive consequences for the device long time reliability). In Fig. 4 for frequencies $f \gtrsim 10$ kHz an ac related EL emerges out of the quasi DC luminescence background. This type of EL—schematically illustrated in Fig. 1(d)—has been invented by Walters *et al.*[5] as a field effect driven mechanism. The luminescence intensity increases with increasing number of switching cycles up to 100–500 kHz and collapses at 1 MHz AC signal frequency. The highest EL intensity occurs at much higher AC frequencies than obtained by Walters *et al.*.[5] or predicted by Carreras *et al.*[13] ($f \leq 50$ kHz). Here, the gate capacitive charging time constant is clearly reduced due to our very small transistor. In addition the 2 nm thin direct tunneling oxide enables higher charging currents with shorter charging times (as confirmed by their memory device characteristics)[10,11] in comparison to FN tunneling as reported by Walters *et al.*[5] where the NCs are located closer to the oxide center. The dependence of the EL intensity maximum on the ac voltage amplitude reveals the significance of the charge transfer rate. The EL quenches at about $f = 1$ MHz which corresponds supposedly to the physical limit of radiative recombination of excitons in tiny Si NCs, i.e., their radiative lifetime.[5,13]

In conclusion, very small (20×20 μm^2) Si NC based light emitting nMOSFET devices are demonstrated where charge carriers are injected into NCs by direct tunneling, not by FN tunneling as in devices reported so far. The direct tunneling leads to a faster device operation which was proven by EL at one order of magnitude higher ac frequencies. Another advantage of direct tunneling is the lower operation voltage and the reduced oxide degradation which increases the device life time. The direct tunneling distances are achieved by a self-alignment process which yields an additional NC layer leading to a further increase of luminescence.

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