Register Base +	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**direction**	usage	**default**	remarks
0x100C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read / write**	time-bomb disable		
0x1050	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read only**	port A status		
0x1054	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read only**	port B status		
0x1058	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read only**	port C status		
0x105C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read only**	port D status		
0x1060	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read only**	port E status		
0x1064	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read only**	port F status		
0x1018	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read / write**	mask for ports A[31] downto A[0]	**0x00000000**	bitwise; 0 means inhibit
0x101C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read / write**	mask for ports B[31] downto B[0]	**0xFFFFFFFF**	bitwise; 0 means inhibit
0x1020	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read / write**	mask for ports C[31] downto C[0]	**0xFFFFFFFF**	bitwise; 0 means inhibit
0x1024	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read / write**	mask for ports D[31] downto D[0]	**0x000000FF**	bitwise; 0 means inhibit
0x1028	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read / write**	mask for ports E[31] downto E[0]	**0x000000FF**	bitwise; 0 means inhibit
0x102C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read / write**	mask for ports F[31] downto F[0]	**0xFFFFFFFF**	bitwise; 0 means inhibit
0x1030	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read only**	ID code meazzanine board on port D		(see details)
0x1034	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read only**	ID code meazzanine board on port E		(see details)
0x1038	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read only**	ID code meazzanine board on port F		(see details)
0x1100	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read only**	revision of USER FPGA code	**0x00005207**	(see details)
0x1104	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read / write**	scratch register	**0xDEADBEEF**	test register
0x1108	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read / write**	LED test	**0x00000000**	(see details)
0x110C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read / write**	GEO address	**0x00000000**	
0x1200	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read / write**	control register	**0x00000000**	(see details)
0x1204	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read / write**	trigger downscaling factor	**0x00000001**	
0x1208	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read / write**	manual veto	**0x00000000**	
0x1110	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read / write**	gate 0 width	**0x00000064**	10ns steps
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read / write**	gate 0 delay	**0x00000064**	10ns steps
0x1114	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read / write**	gate 1 width	**0x00000032**	10ns steps
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read / write**	gate 1 delay	**0x00000032**	10ns steps
0x1118	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read / write**	gate 2 width	**0x00000032**	10ns steps
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read / write**	gate 2 delay	**0x00000032**	10ns steps
0x111C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read / write**	gate 3 width	**0x00000032**	10ns steps
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read / write**	gate 3 delay	**0x00000032**	10ns steps
0x1300	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read only**	FIFO status		(see details)
0x2000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**read only**	FIFO data		

ID code mzzanine boards:

lowest 3 bits:	b000 -> board type = A395A
	b001 -> board type = A395B
	b010 -> board type = A395C
	b011 -> board type = A395D

revision

bits 15 downto 12:	setup number
bits 11 downto 8:	major revision number
bits 7 downto 0:	minor revision number

LED test:

bit 0:	0-> OFF; 1-> ON "red LED"
bit 1:	0-> OFF; 1-> ON "green LED"
bit 8:	0-> LEDs controlled by FPGA; 1-> LEDs controlled by User

control register:

bit 0:	reset scalers for busy lengths to 0
bit 3:	reset fifo
bit 4:	input logic for Pla: 0-> AND ; 1->OR
bit 5:	use TDT
bit 6:	double detector logic: 0 -> AND; 1-> OR
bit 8:	enable veto scaler
bit 9:	enable module operation
bit 11:	enable pl_coin production
bit 12:	enable in_or_block1 production
bit 13:	enable in_or_block2 production
bit 14:	enable in_or_block3 production
bit 15:	enable in_or_block4 production

FIFO status

bits 12 downto 0:	FIFO fill level -> number of 32bit words stored in FIFO
bits 15 downto 13:	b000
bit 16:	FIFO full flag
bit 17:	FIFO empty flag
bit 18:	FIFO almost full flag (>= 4000 words in FIFO)
bit 19:	FIFO almost empty flag (< 2 words in FIFO)
bit 31 downto 18:	0xABC

FIFO data

bits 31 downto 27:	GEO
bits 26 downto 25:	id
if id = b00 / b10	<u>Header / Trailer</u>
bits 24 downto 14:	FIFO write counter
bits 13 downto 3:	trigger counter
bits 2 downto 0:	b111
if id = b01	<u>Data word</u>
bits 24 downto 22:	word id
bit 21:	range id
bits 20 downto 16:	b00000
bits 15 downto 0:	data

word id	range id	data		
b000	b0	bits 15 downto 0 of	busy_00	QDC1 Busy
	b1	bits 31 downto 16 of	busy_00	
b001	b0	bits 15 downto 0 of	busy_01	QDC2 Busy
	b1	bits 31 downto 16 of	busy_01	
b010	b0	bits 15 downto 0 of	busy_02	
	b1	bits 31 downto 16 of	busy_02	
b011	b0	bits 15 downto 0 of	busy_04	TDT
	b1	bits 31 downto 16 of	busy_04	
b100	b0	bits 15 downto 0 of	trigger	
	b1	bits 31 downto 16 of	trigger	
b101	b0	bits 15 downto 0 of	veto	
	b1	bits 31 downto 16 of	veto	
b110	b0	bits 15 downto 0 of	man. veto	
	b1	bits 31 downto 16 of	man. veto	

Input A		used for
0		
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		
20		
21		
22		
23		
24		
25		
26		
27		
28		
29		
30		
31		

Input B		used for
0	in_1_00	double detector 1 PMT 1
1	in_1_01	double detector 2 PMT 1
2	in_1_02	double detector 3 PMT 1
3	in_1_03	double detector 4 PMT 1
4	in_1_04	double detector 1 PMT 2
5	in_1_05	double detector 2 PMT 2
6	in_1_06	double detector 3 PMT 2
7	in_1_07	double detector 4 PMT 2
8	in_2_00	single detector
9	in_2_01	
10	in_2_02	
11	in_2_03	
12	in_2_04	
13	in_2_05	
14	in_2_06	
15	in_2_07	
16	in_3_00	
17	in_3_01	
18	in_3_02	
19	in_3_03	
20	in_3_04	
21	in_3_05	
22	in_3_06	
23	in_3_07	
24	busy_04	TDT
25	busy_05	
26	busy_06	
27	busy_07	
28	misc_00	FPGA 2 C0 (LNE)
29	misc_01	
30	misc_02	
31	misc_03	SOR

Output C		used for
0	in_or_00-07	Scaler
1	in_or_08-15	Scaler
2	in_or_16-19	Scaler
3	in_or_20-23	Scaler
4	pl_coin_0	Scaler
5	pl_coin_1	Scaler
6	global_or	Scaler
7	trigger_raw	Scaler
8	trigger	Scaler
9	trigger_ds	Scaler
10	LCLK	Scaler
11	LCLK_and veto	Scaler
12	LCLK_and_nveto	Scaler
13	veto	Scaler
14	not veto	Scaler
15	1	Scaler
16	coin(0)	Scaler
17	coin(1)	Scaler
18	coin(2)	Scaler
19	coin(3)	Scaler
20		Scaler
21		Scaler
22		Scaler
23		Scaler
24		Scaler
25		Scaler
26		Scaler
27		Scaler
28		Scaler
29		Scaler
30		Scaler
31	misc_03	Scaler

Input D		used for
0	busy_00	QDC1 Busy
1	busy_01	QDC2 Busy
2	busy_02	
3	busy_03	
4	pl1_01	
5	pl1_02	
6	pl2_01	
7	pl2_02	

Output E		used for
0	gate_0	
1	gate_1	
2	gate_2	
3	gate_3	
4	trigger	G&D Gen.
5	veto	
6	nveto	
7	busy_04	

Output F		used for
0	trigger_ds	T1
1	forced trigger	T2
2	not veto	
3	1	
4	gate_0	TDC TRG
5	gate_1	
6	gate_2	
7	gate_3	
8	gate_0	TDC in
9	trigger	TDC in
10	veto	TDC in
11	not veto	TDC in
12	gate_0	
13	trigger	
14	veto	
15	not veto	
16	in_1_00	
17	in_1_01	
18	in_1_04	
19	in_1_05	
20	in_2_00	
21	in_2_00	
22	coin(0)	
23	coin(1)	
24	in_or_00-07	
25	in_or_08-15	
26	global_or	
27	trigger_raw	
28	busy_00	
29	busy_04	
30	misc_03	
31	mult_win	

Output G	
0	trigger
1	veto

LED:
Red on <=> (veto == 1)
Green on <=> (trigger == 1)