

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 688072

## Research and Innovation Action (RIA)

## **IONS4SET**

Project title:	Ion-irradiation-induced Si Nanodot Self- Assembly for Hybrid SET-CMOS Technology
Project coordinator:	Helmholtz-Zentrum Dresden-Rossendorf e.V., Dresden, Germany
HZDR participant:	Institute of Ion Beam Physics and Materials Research
Starting date: Duration (months):	01.02.2016 48

## Summary

Billions of tiny computers that can sense and communicate from anywhere are coming online, creating the "Internet of Things" (IoT). As the IoT continues to expand, more and more devices need batteries and plugs. According to Gartner (www.gartner.com), there will be nearly 26 billion devices connected to the IoT by 2020. Therefore, together with improved batteries, advanced computation and communication must be delivered at extremely low-power consumption.

It is well-known that Single Electron Transistors (SET) are extremely lowenergy dissipation devices. CMOS and SETs are complementary: SET is the champion of low-power consumption while CMOS advantages like highspeed, driving etc. compensate exactly for SET's intrinsic drawbacks. Unrivalled integration with high performance is expected for hybrid SETCMOS architectures.

Manufacturability is the roadblock for large-scale use of hybrid SET-CMOS architectures. To assure room temperature (RT) operation, single dots of diameters below 5 nm have to be fabricated, exactly located between source and drain with tunnel distances of a few nm. A reliable CMOS compatible process of co-fabrication of RT-SETs and FETs is not yet available.

IONS4SET will pave the way for fabrication of low-energy devices operating at RT using the discovery of a bottom-up selfassembly process. Lithography cannot deliver the feature sizes of 1...3 nm required for RT operation. IONS4SET will provide both, (i) controlled self-assembly of single ~ 2 nm Si dots and (ii) self-alignment of each nanodot with source and drain at tunneling distances of ~ 2 nm.

The fabrication process of the Si nanodot involves (i) ion irradiation through a few tens of nm thin Si pillars with an embedded SiO2 layer and (ii) thermal activation of self-assembly. Dot self-assembly works for narrow pillars only, i.e. nanopillar fabrication is crucial for IONS4SET. Finally, a power saving hybrid SET/CMOS device with a vertical gate-all-around nanowire GAA-SET will be fabricated.

