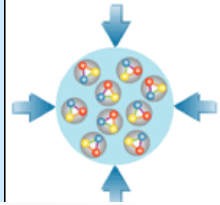


Laboratory test setup for N-XYTER chips and Si detectors

Adam Czermak

Institute of Nuclear Physics PAS,
Krakow, Poland

OUTLINE

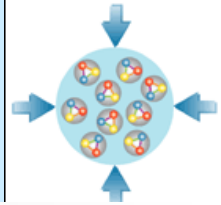
- Overview of the Test Setup,

  Based on SUCIMA;

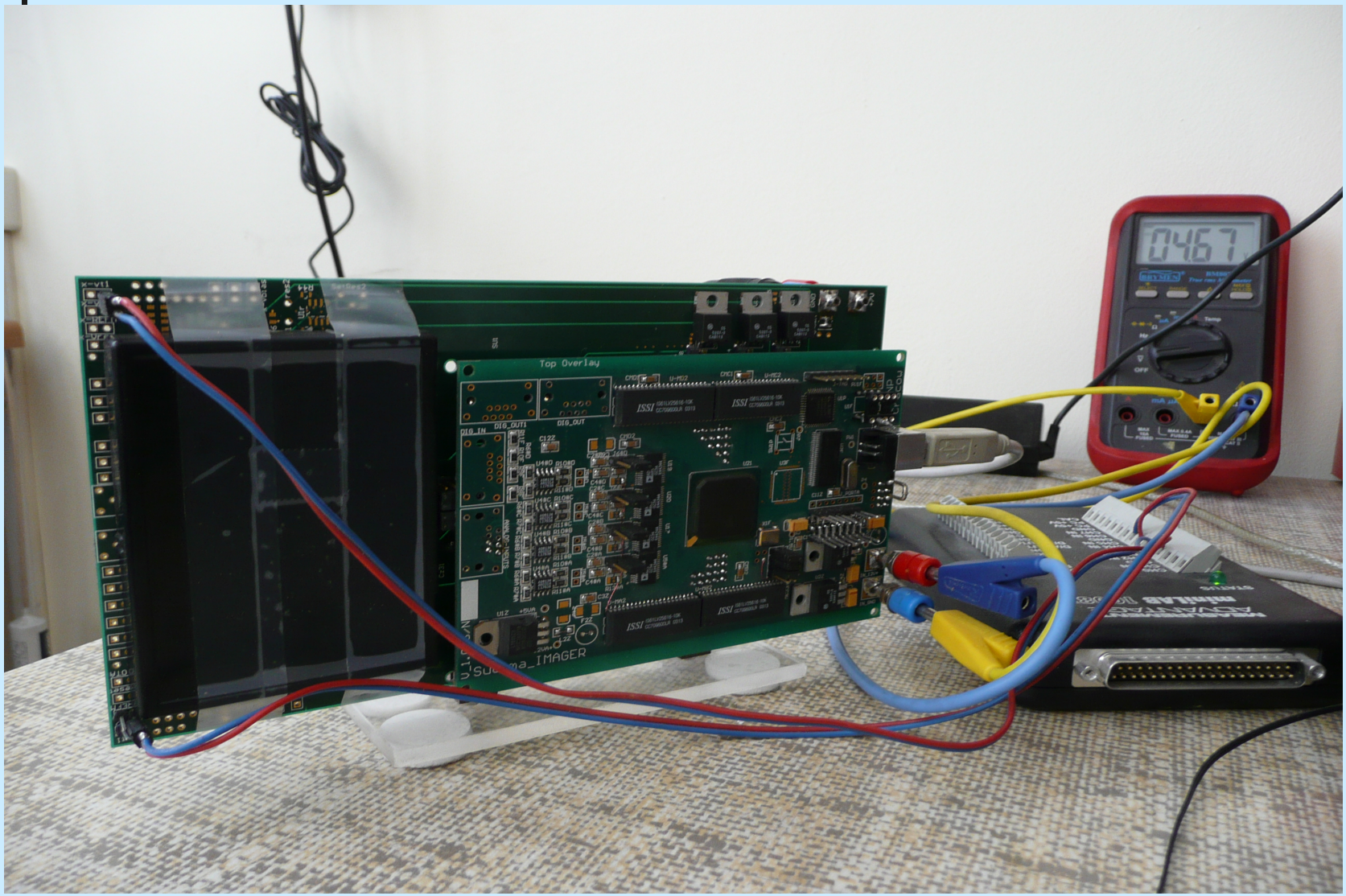
  Silicon Ultra Fast Cameras for Electron and Gamma

  Sources In Medical Application
- Test setup for MSGCROC and N-XYTER ASICs
- Test results from some initial tests of two n_XYTER chips performed in Krakow.
- Conclusion
- Next steps - towards N-XYTER tests.

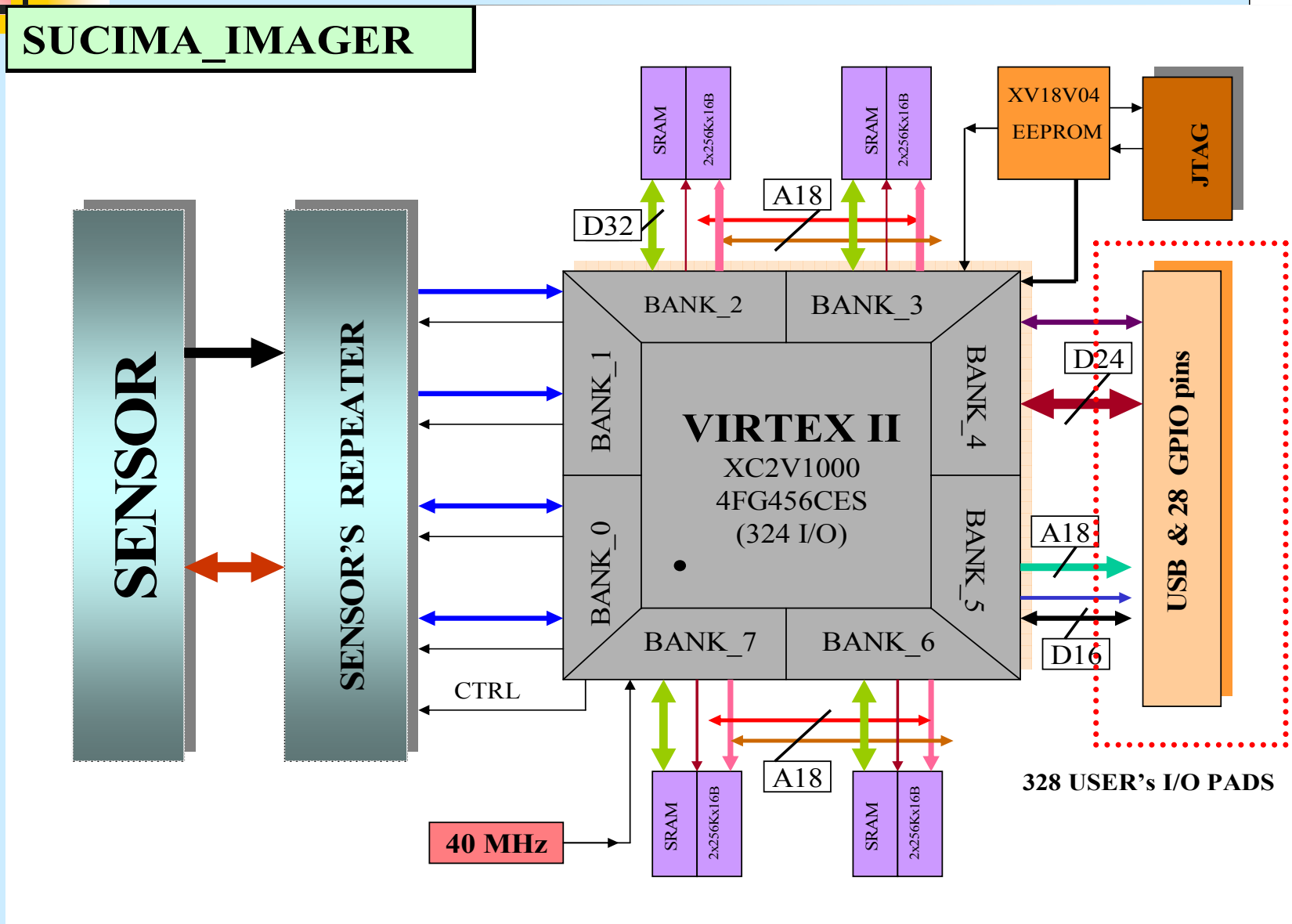
Laboratory test setup for N_XYTER



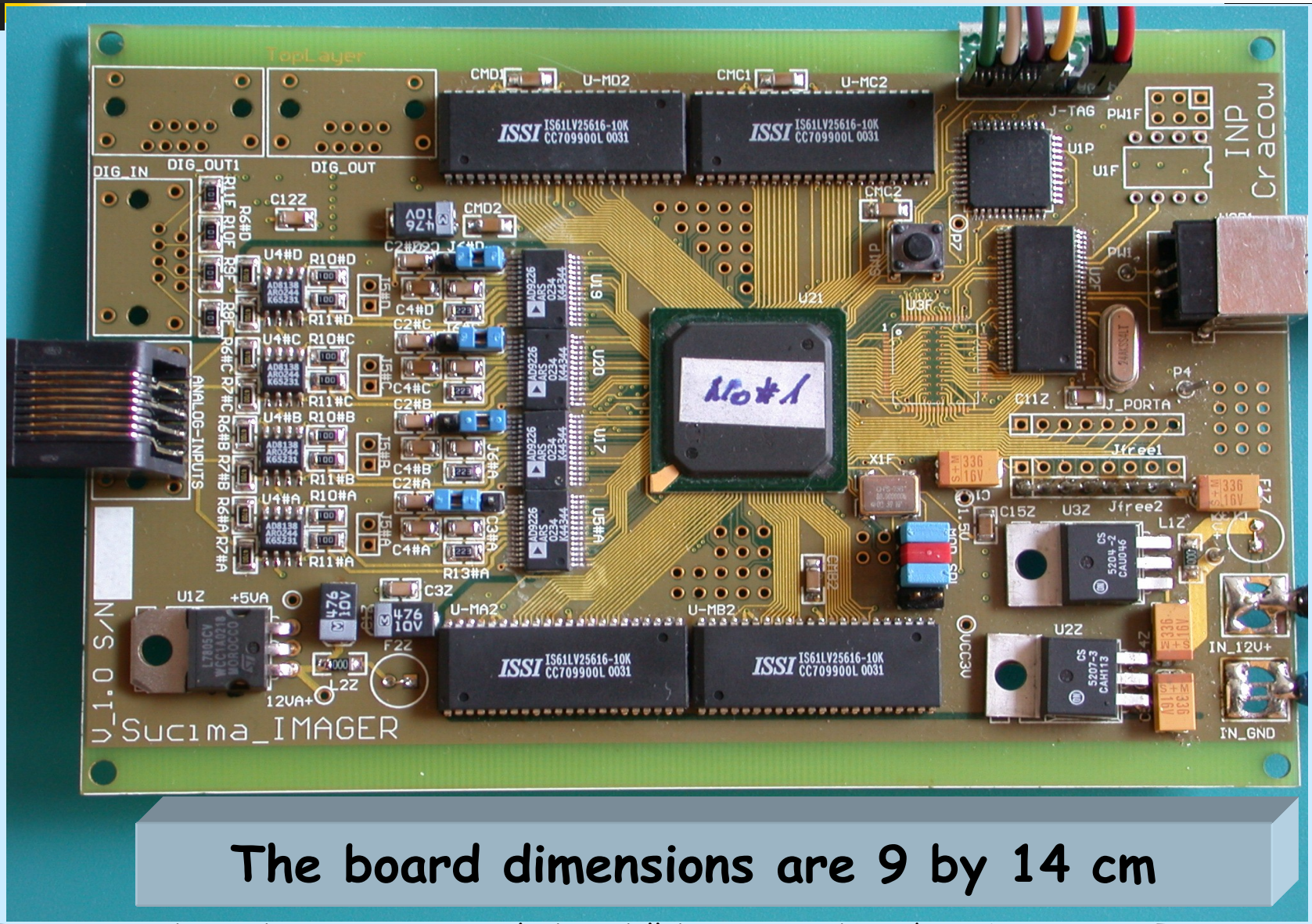
- The main goal of this setup is to have laboratory user-friendly test setup for all foreseen to be performed tests of DETNI & CBM Collaborations VLSI chips developed for MSGC and Si Detectors.
- All laboratories involved in these tests should be able to adopt the system to their specific needs using NI_LabView and Xilinx_ISE software.
- The first evaluation PCB for 2 N-XYTER chips and Si detector as an interface to SUCIMA Imager module has been designed and is beeing produced in ILFA.


Top Overlay
0467

SUCIMA_Imager Architecture

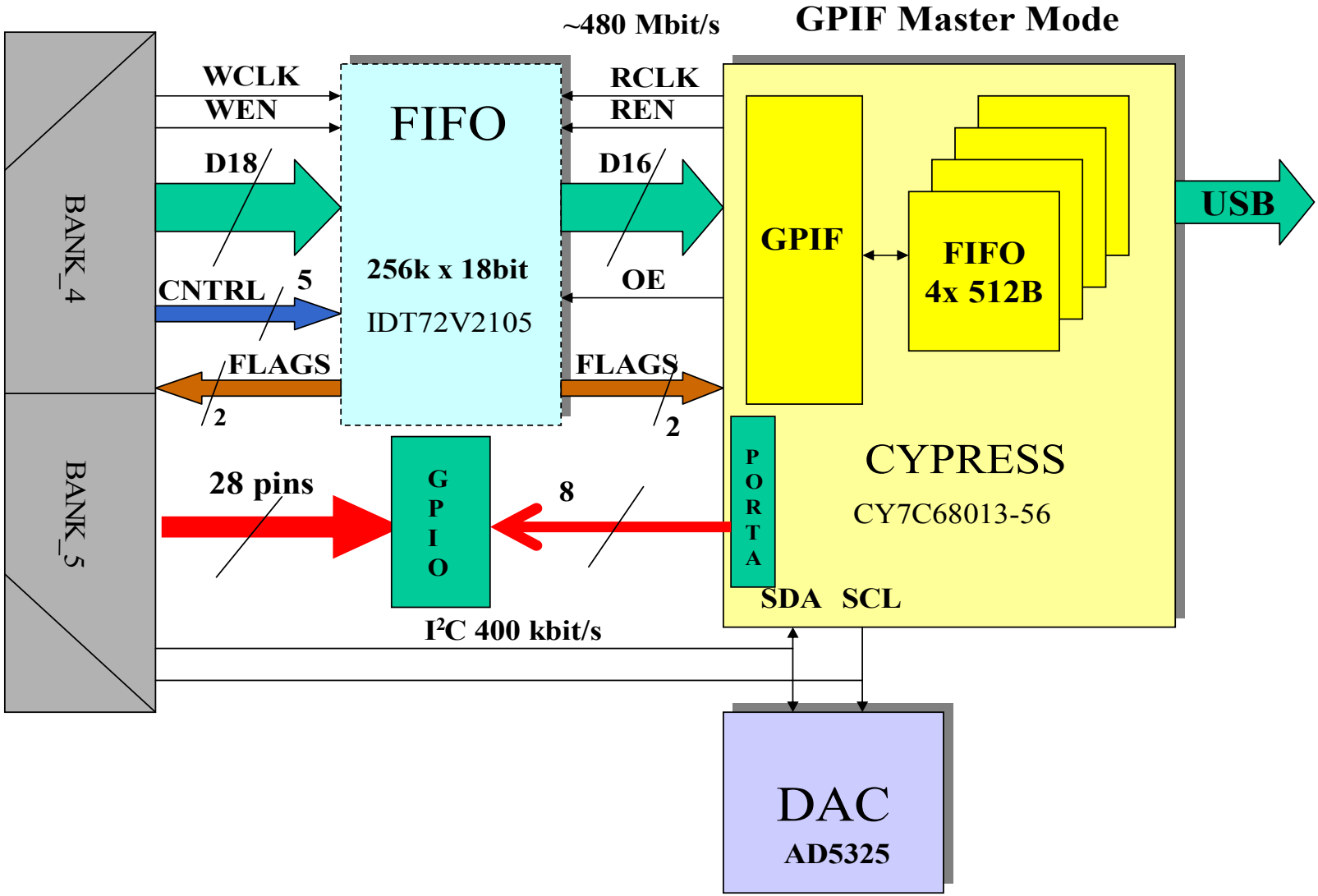


SUCIMA_Imager PCB card

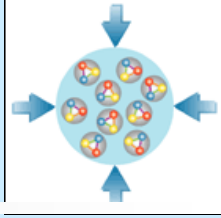


The board dimensions are 9 by 14 cm

SUCIMA_Imager connectivity to PC

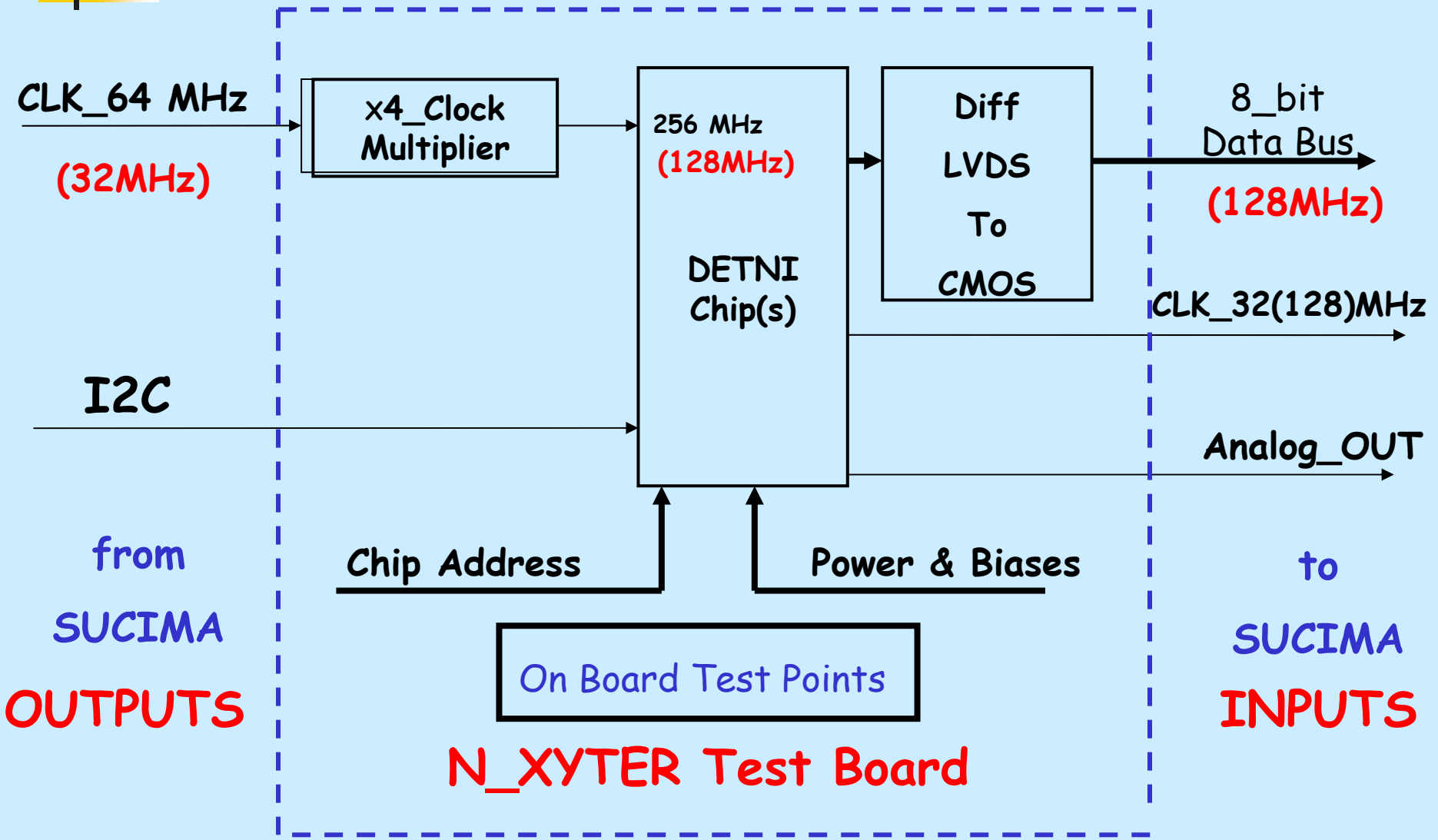


SUCIMA_Imager DAQ key parameters

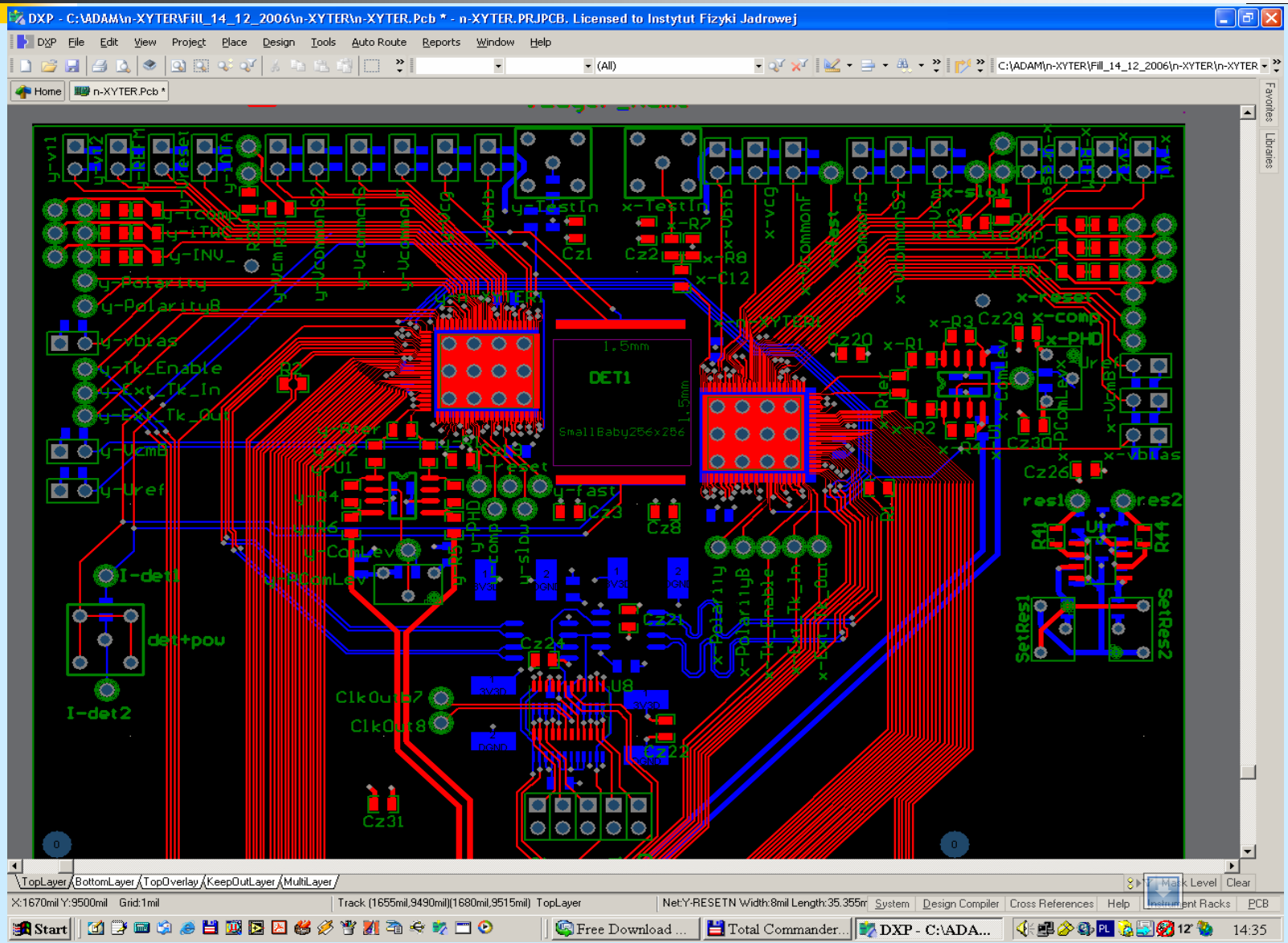


- 4 independent analogue input channels with 12 bit pipeline ADCs @ 65 MSPS.
- Each channel equipped with 256 K of 32 bit fast Static RAM memories.
- FIFO memory 256 K of 18 bit, can serve as the output buffer (Derandomizer).
- High-speed USB 2.0 port for communication and fast data transfer to/from a PC computer.
- Additional 8 bit Parallel GPIO Port and I2C Port for external devices programming and communication.
- Easy to implement Data_Driven_DAQ_System

N_XYTER CHIP(s) Interface Board

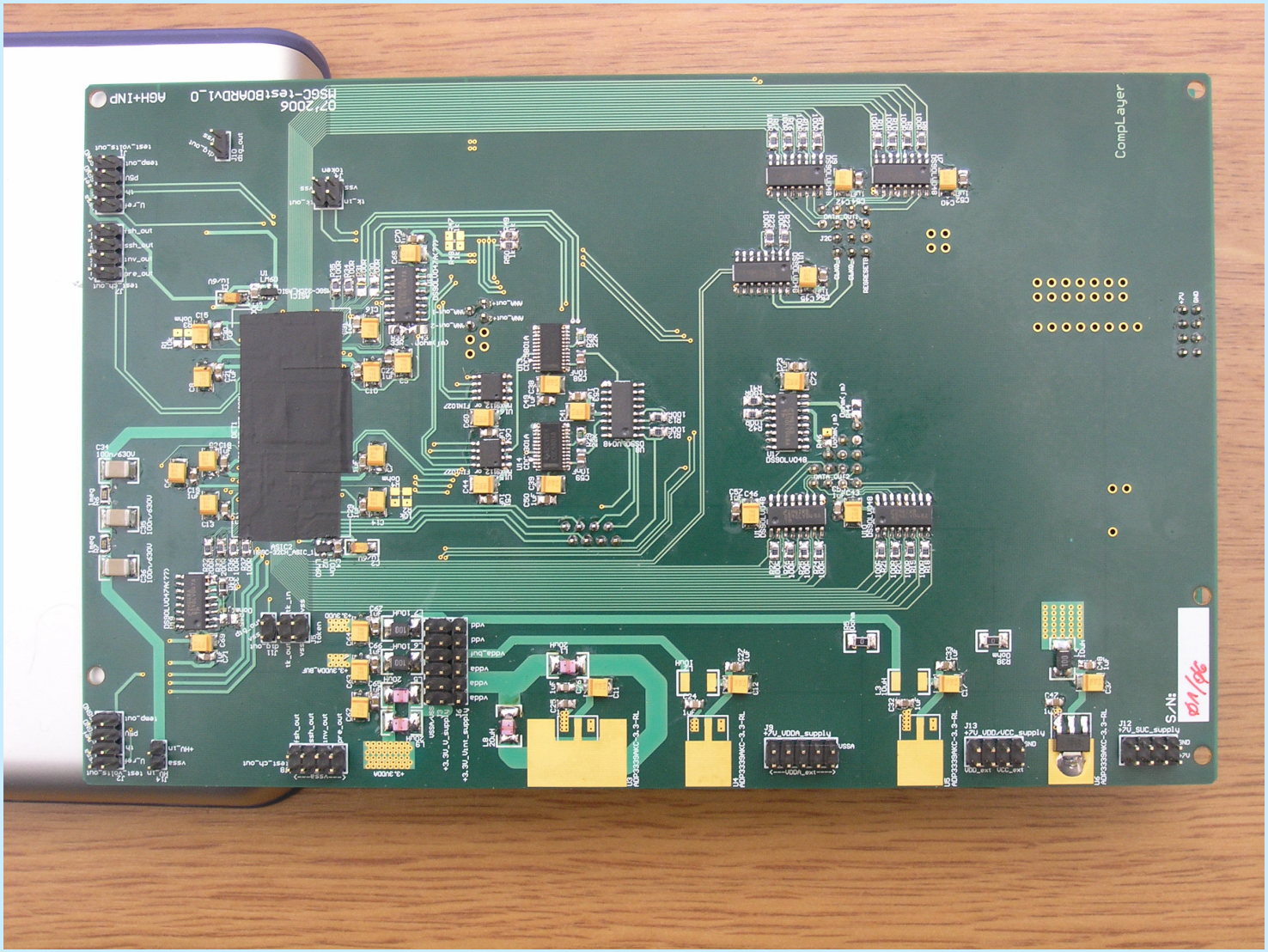


N_XYTER evaluation PCB layout

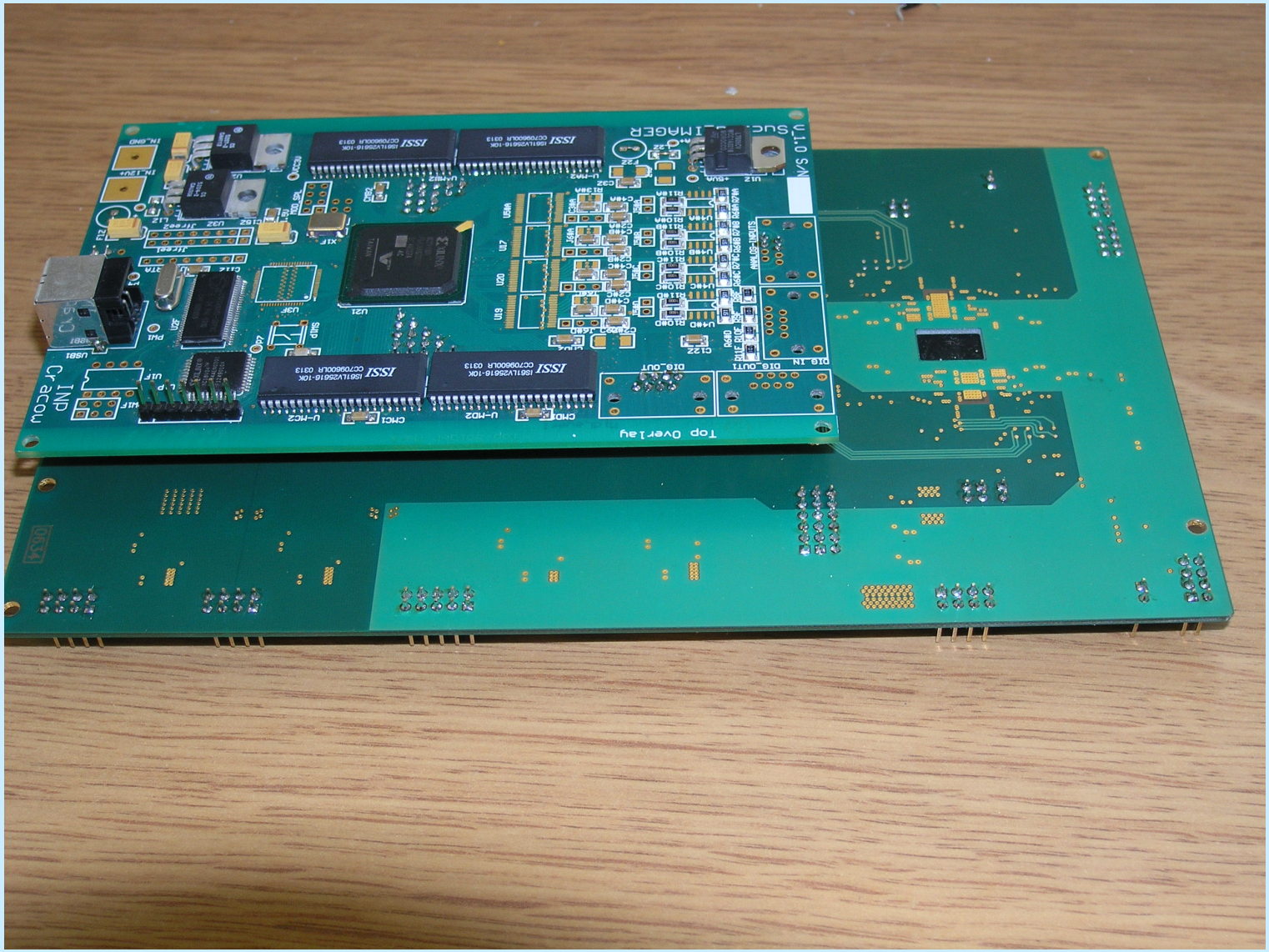


N_XYTER Interface PCB

PCB for MSGC Chips (already operational)



Test Board with SUCIMA_Imager

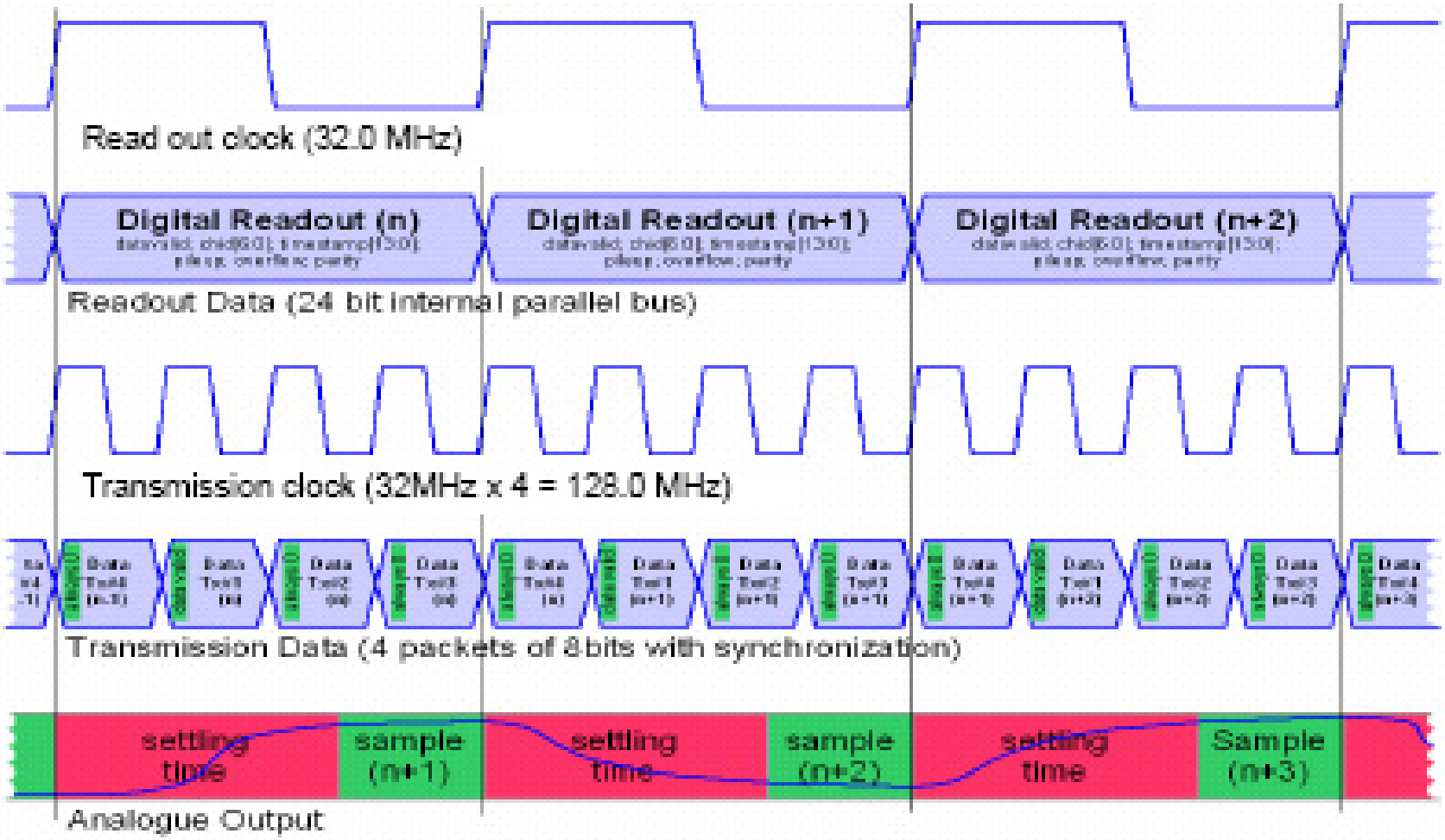


Multiplexed ASICs 8-bit digital data output format

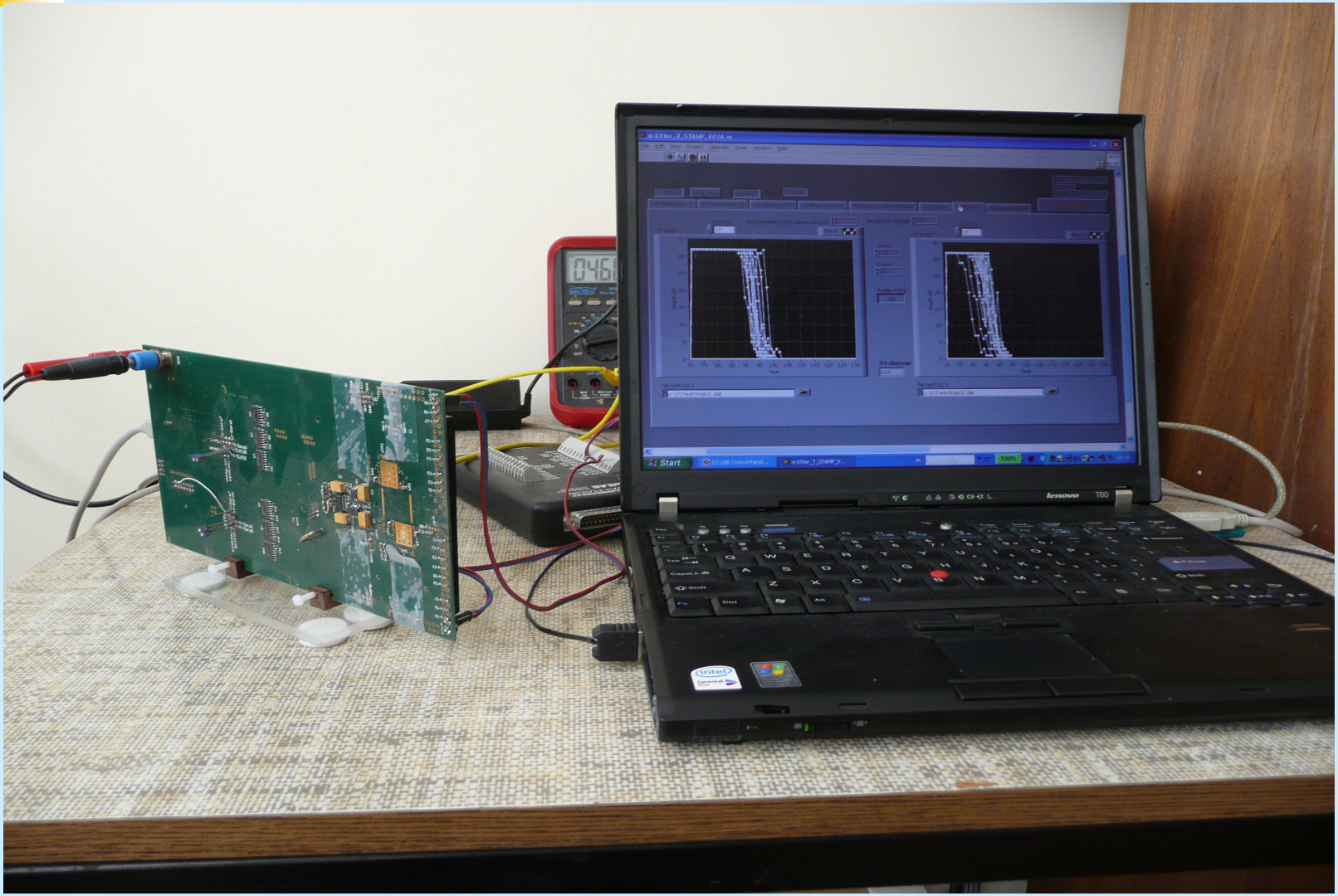
MSGC		Bits							
		7	6	5	4	3	2	1	0
Packets	0	DV1	0	0	TS11	TS10	TS9	TS8	TS7
	1	0	TS6	TS5	TS4	TS3	TS2	TS1	TS0
	2	0	0	0	(ID4)	ID3	ID2	ID1	ID0
	3	0	0	0	0	0	PileUp	OverF	Parity

Si-MSD GEM		Bits							
		7	6	5	4	3	2	1	0
Packets	0	DV1	TS13	TS12	TS11	TS10	TS9	TS8	TS7
	1	0	TS6	TS5	TS4	TS3	TS2	TS1	TS0
	2	0	ID6	ID5	ID4	ID3	ID2	ID1	ID0
	3	0	0	0	0	0	PileUp	OverF	Parity

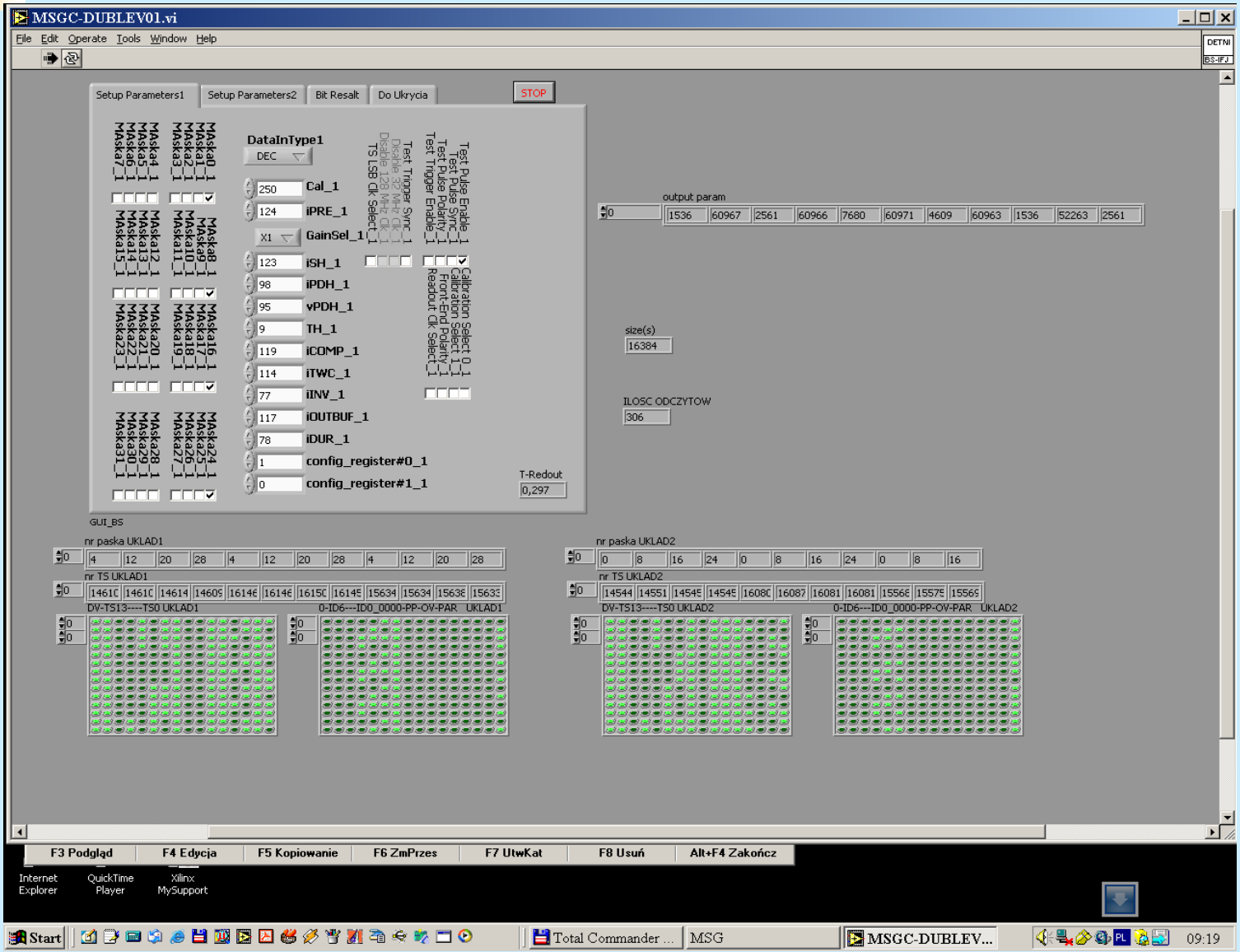
Timing diagram for multiplexed ASIC readout



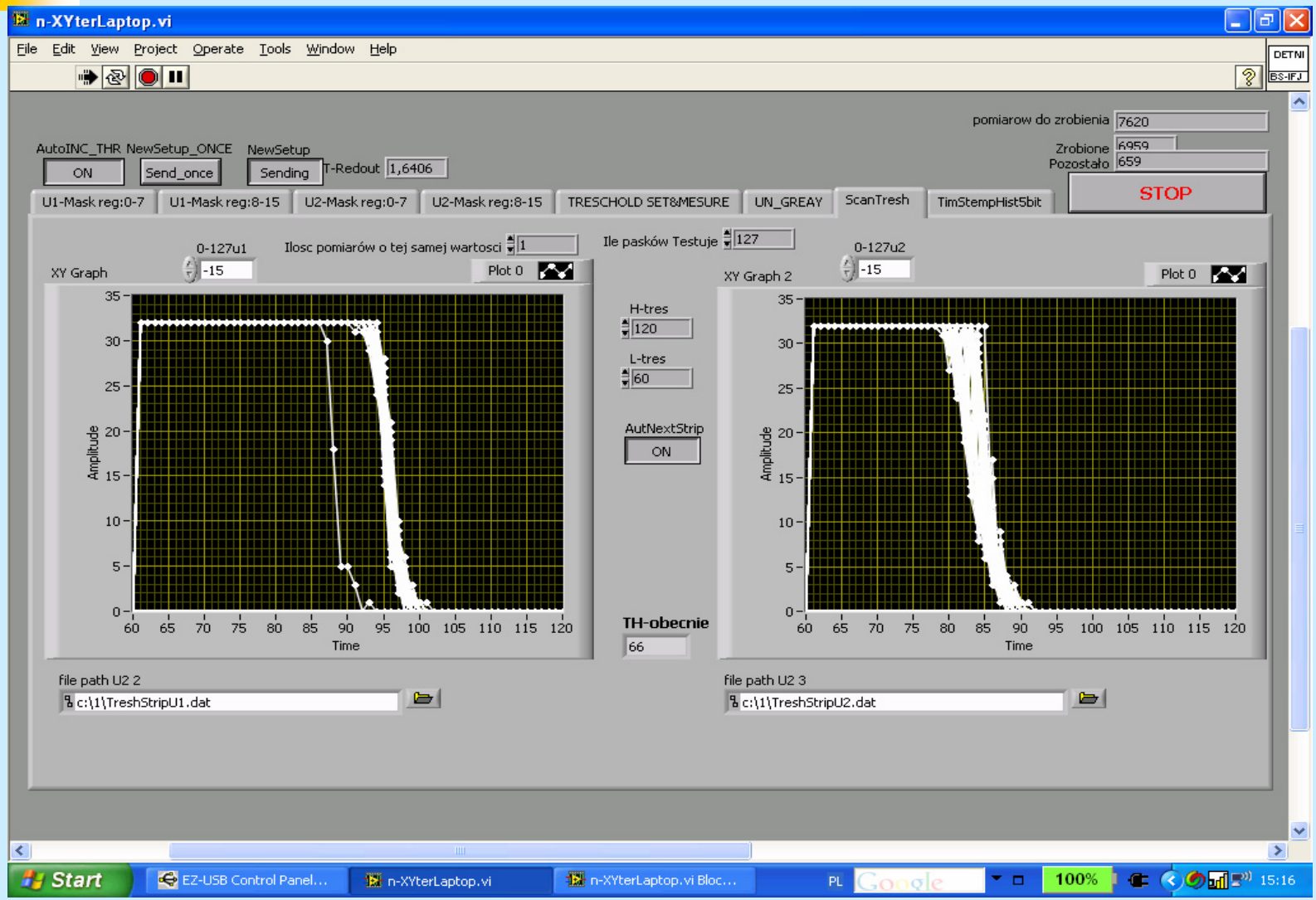
N_XYTER_TEST_SETUP



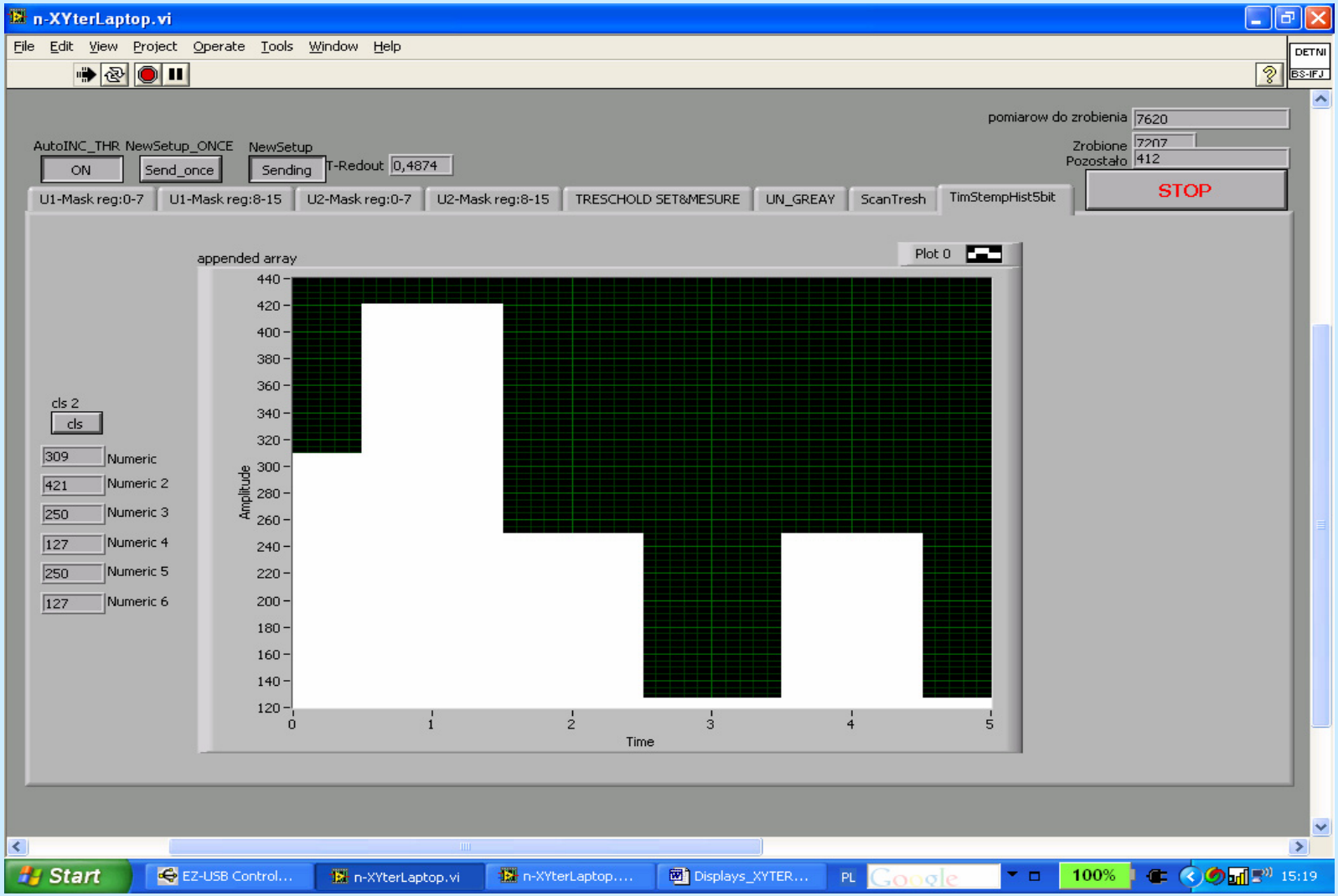
Graphical User Interface



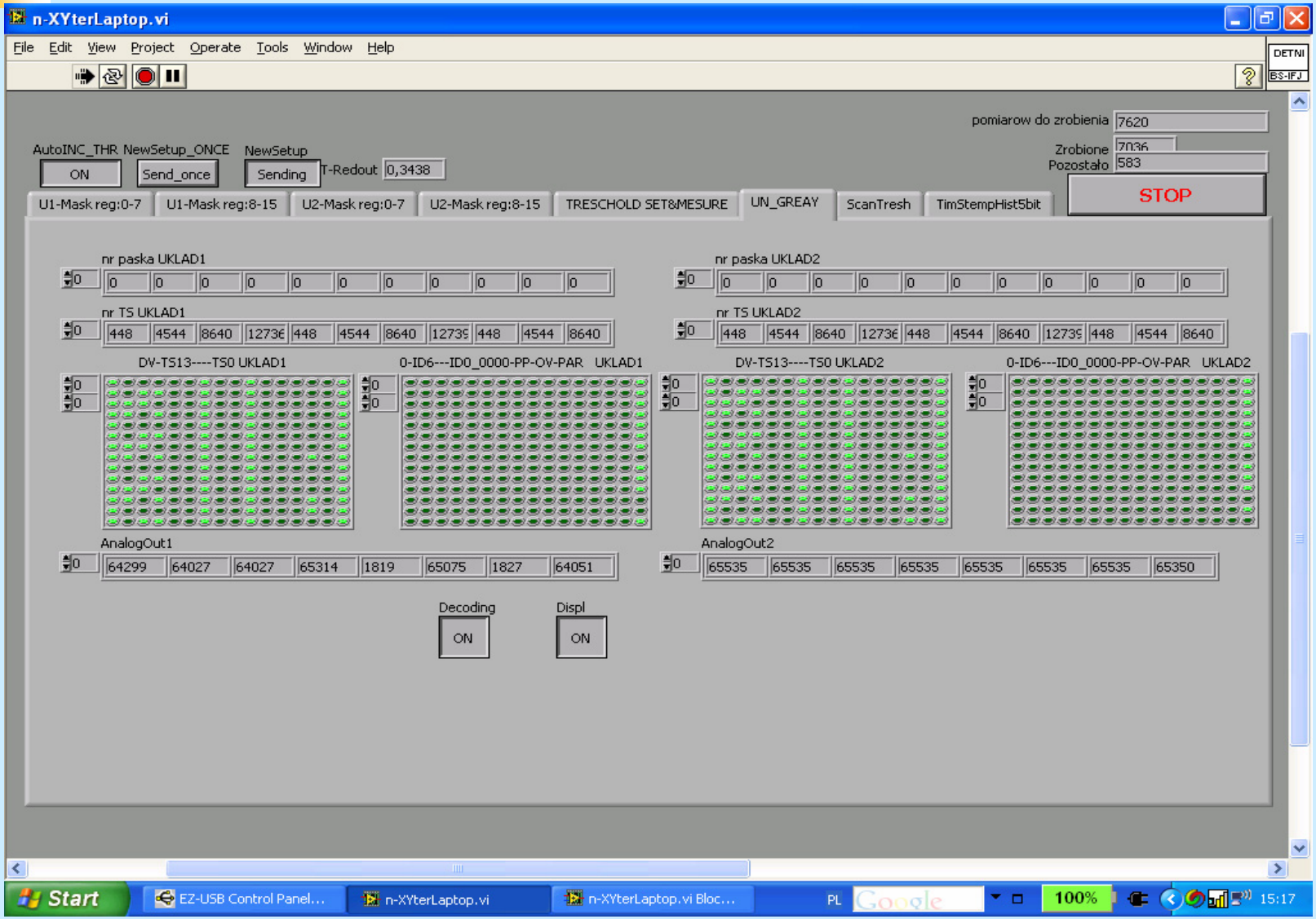
SCAN TRESHOLD GUI



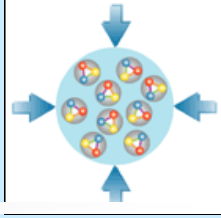
TS_GUI


n-XYterLaptop.vi
File Edit View Project Operate Tools Window Help
DETNI
BS-IFJ
pomiarow do zrobienia 7620
Zrobione 7207
Pozostało 412
AutoINC_THR NewSetup_ONCE NewSetup
ON
Send_once
Sending
T-Redout 0,4874
STOP
U1-Mask reg:0-7
U1-Mask reg:8-15
U2-Mask reg:0-7
U2-Mask reg:8-15
TRESCHOLD SET&MESURE
UN_GREAY
ScanTresh
TimStempHist5bit
appended array
Plot 0
Amplitude
Time
cls 2
cls
309 Numeric
421 Numeric 2
250 Numeric 3
127 Numeric 4
250 Numeric 5
127 Numeric 6
Start
EZ-USB Control...
n-XYterLaptop.vi
n-XYterLaptop....
Displays_XYTER...
PL
100%
15:19

Principles of GUI

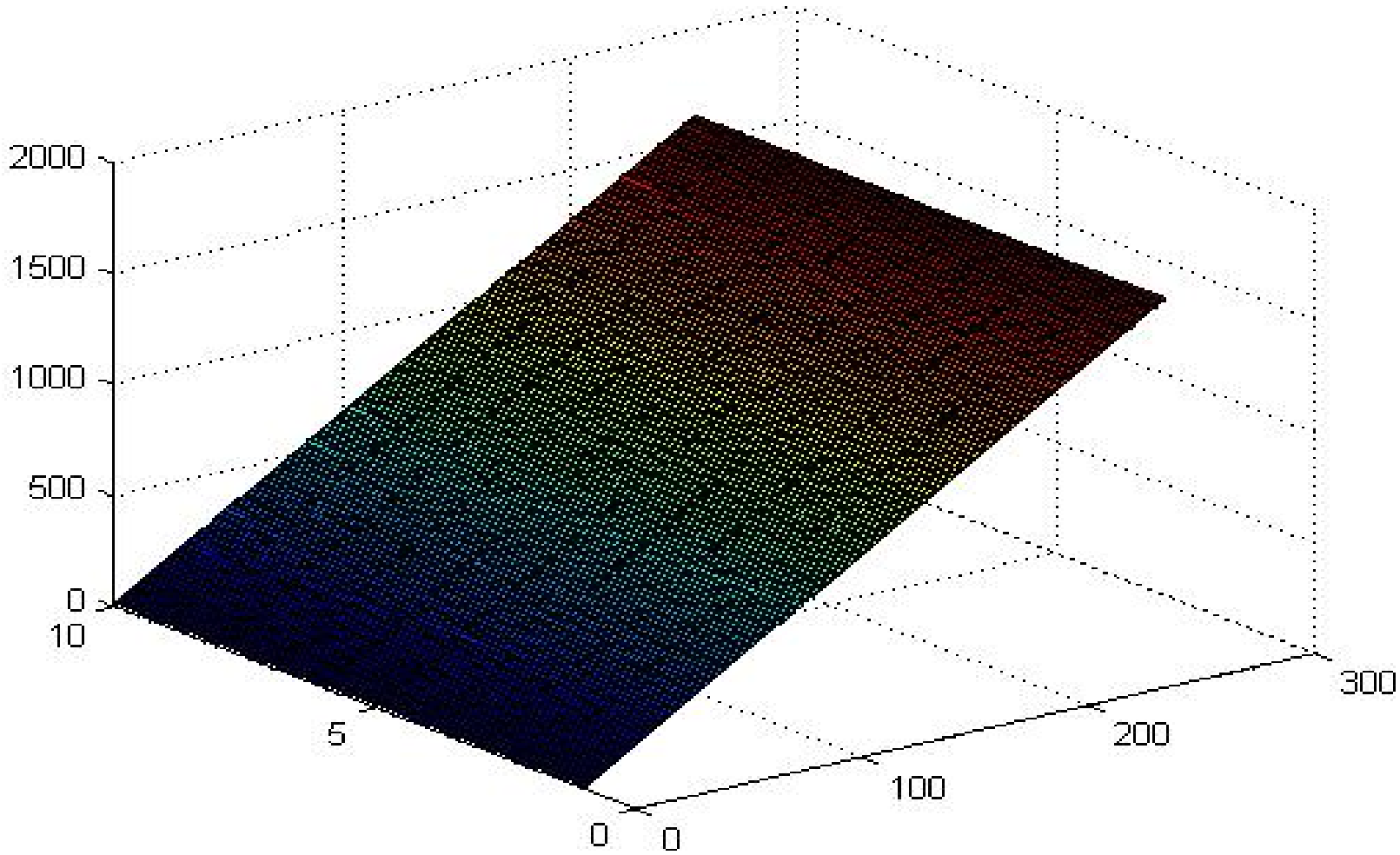


Test Measurements

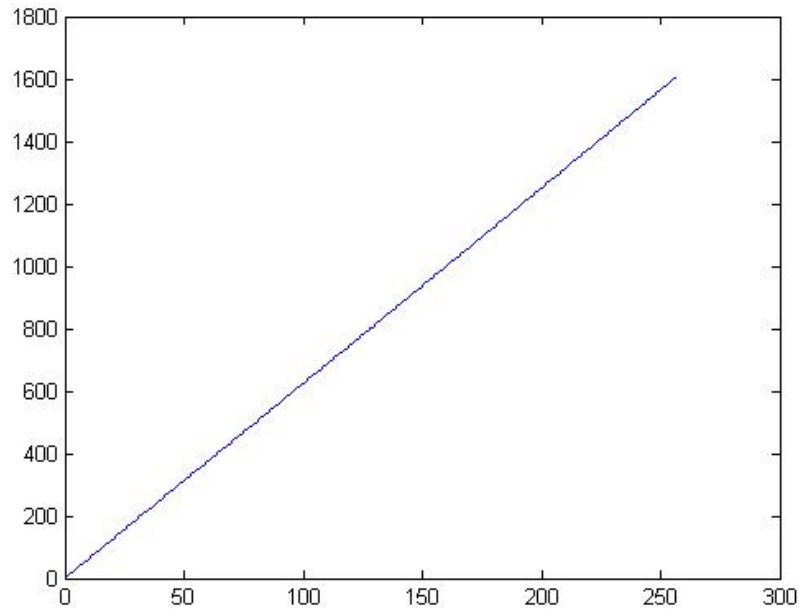


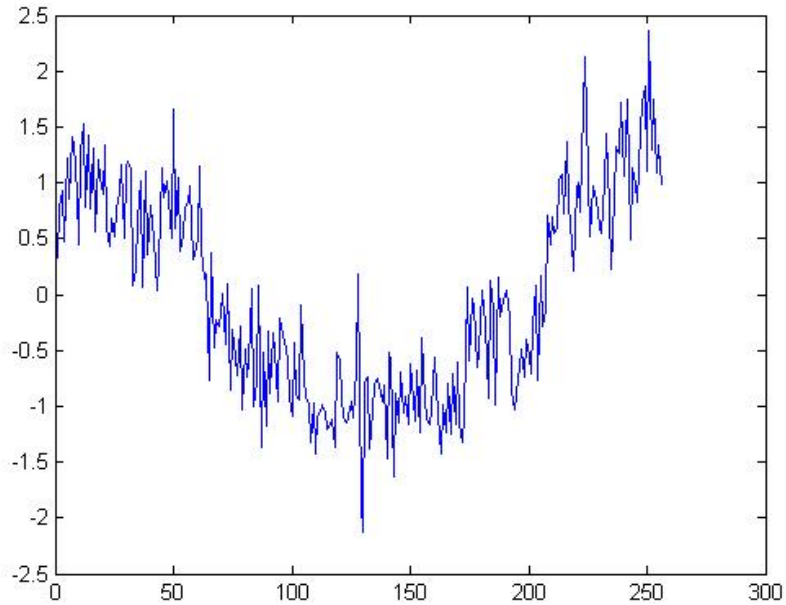
All measurements have been performed at nominal power supply voltage of 3.3 V and nominal bias currents controlled by internal Digital-to-Analog-Converters (DACs).

V_teesh_DAC_Scan



Response curve and integral nonlinearity of the threshold DAC



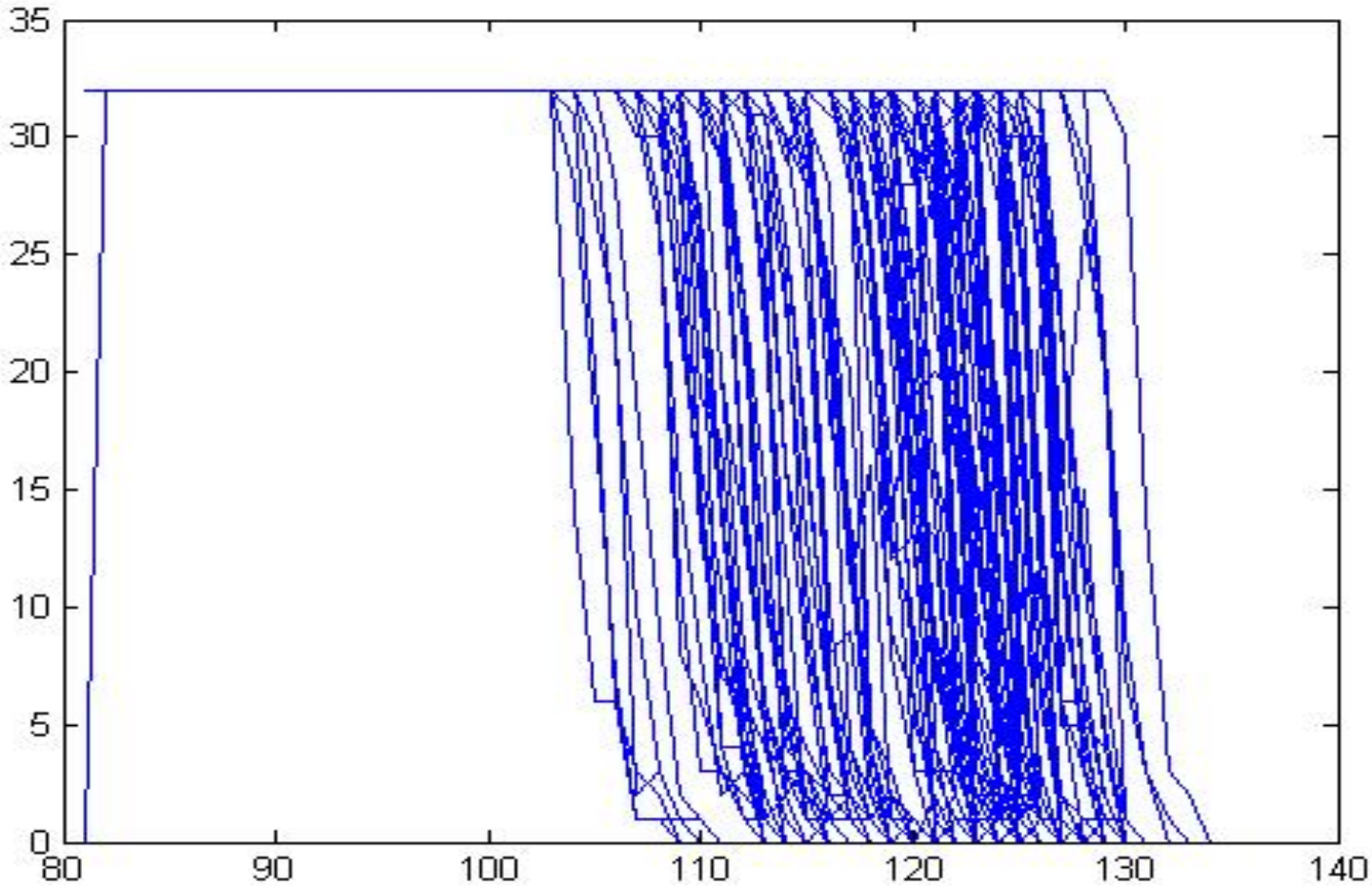


V_Tresd=f(Value_tresh_DAC)

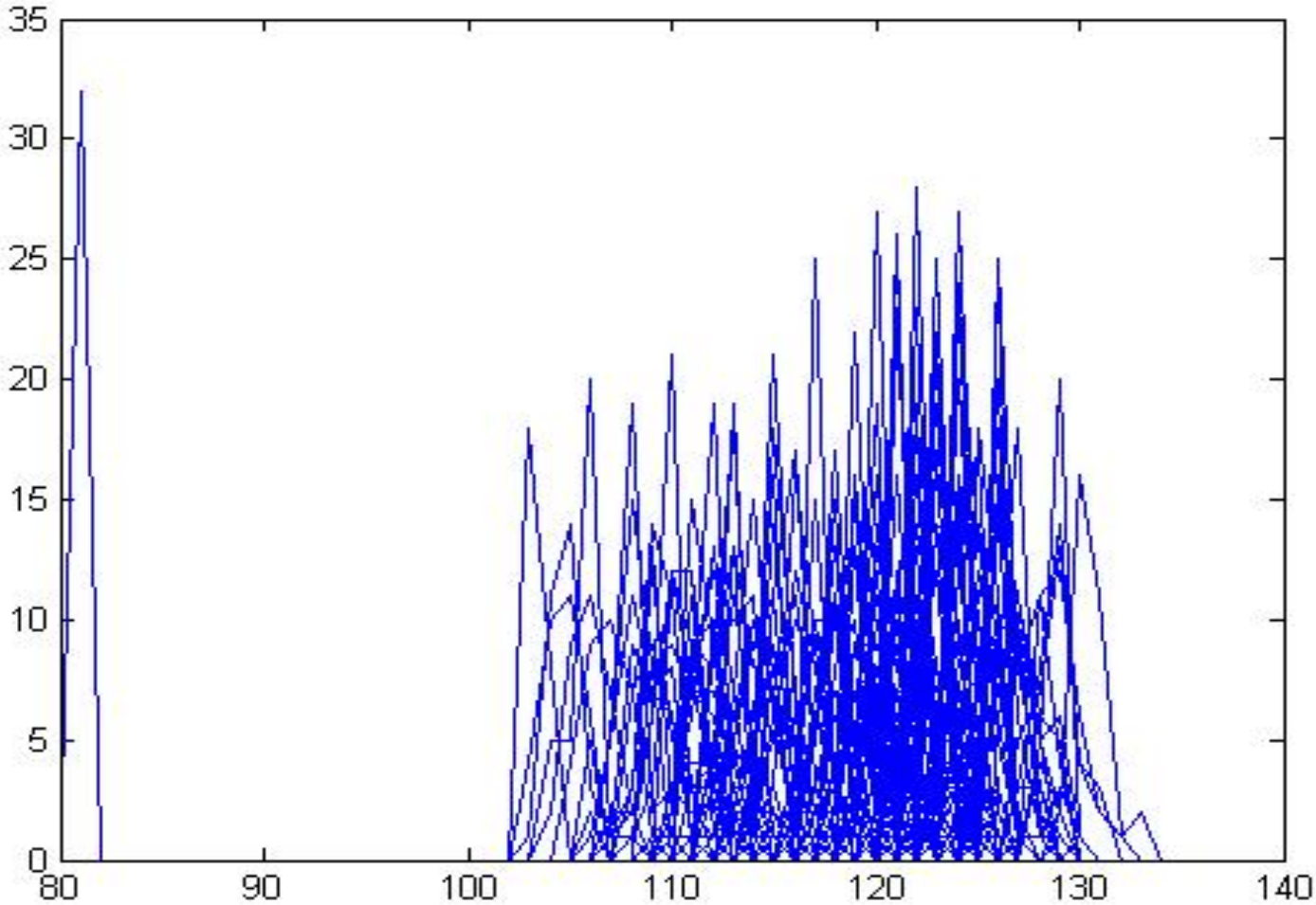
Integral_nonlinarity= f(Value_tresh_DAC)

(Resolution = 11Bits)

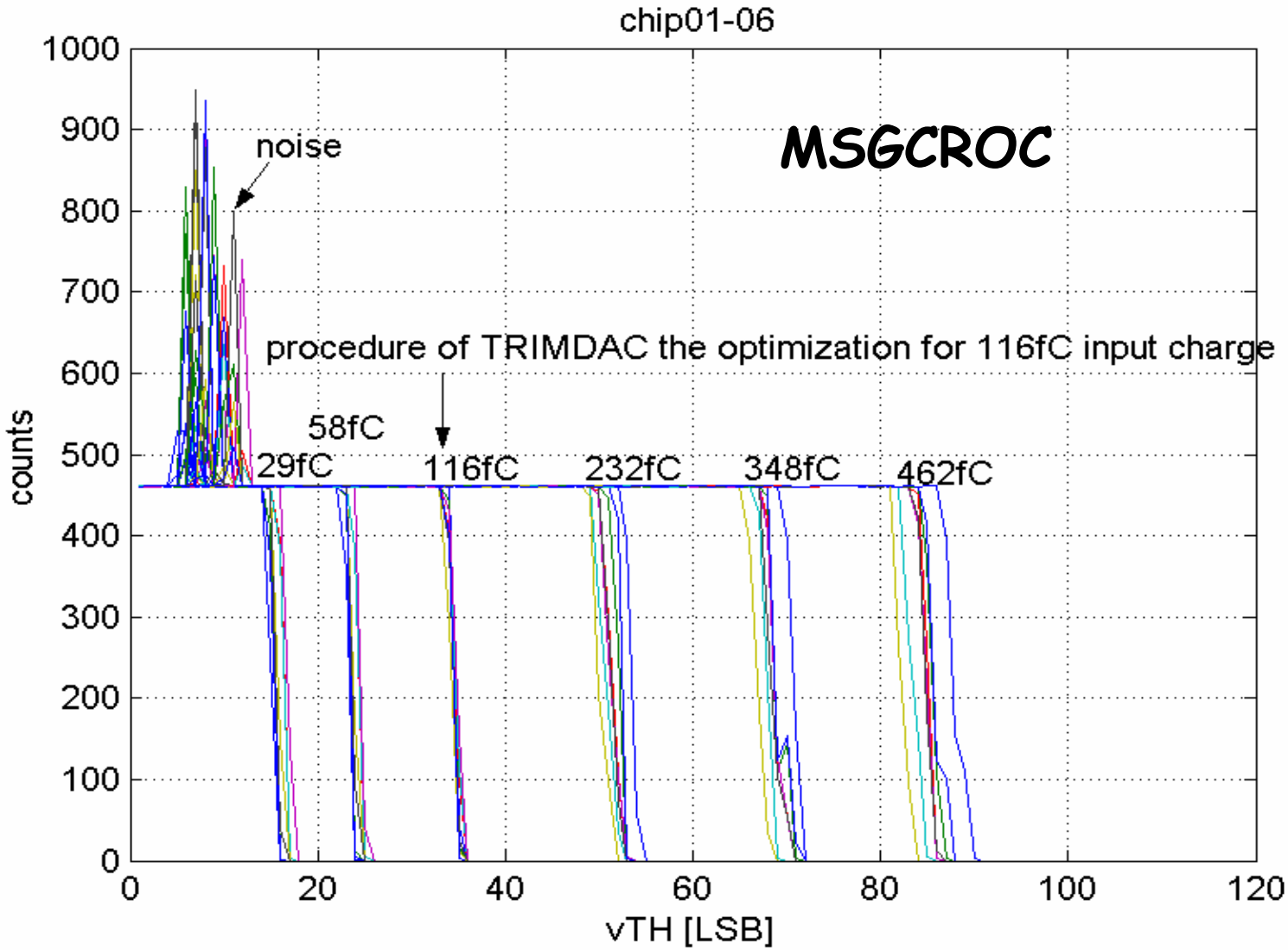
Treshold_Voltage Scan for 128 channels



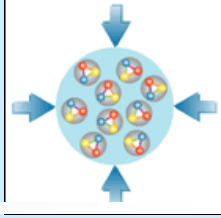
Differentiated S curves



Trigger efficiency vs. threshold for different input charges after trimming the threshold

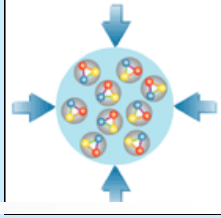


Conclusions



- The tests performed on two N_XYTER ASICs demonstrate functionality of all building blocks on the Chip (CLK ->128 MHz).
- The critical digital circuits responsible for data derandomization and zero suppression, token-based readout have been tested and work correctly.
- There are no indications that the ASIC should not perform correctly at higher clock frequencies (CLK->256 MHz).

Tests to be done in the near future



- Test whether the analogue parameters, i.e. gain, noise and matching of parameters are in agreement with the design specifications.
- Test of the Time Stamp resolution.
- In the near future tests of two chips connected to Si strip detector.
- Tests of the Analog_outputs.
- Power of the Chip vs CLK_freq.