Radiation Hardness Test Chip

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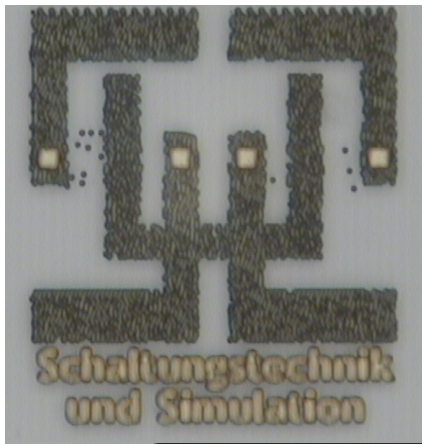
Overview

1. Reminder: Radiation Damage & Remedies
2. Chip description
3. First results

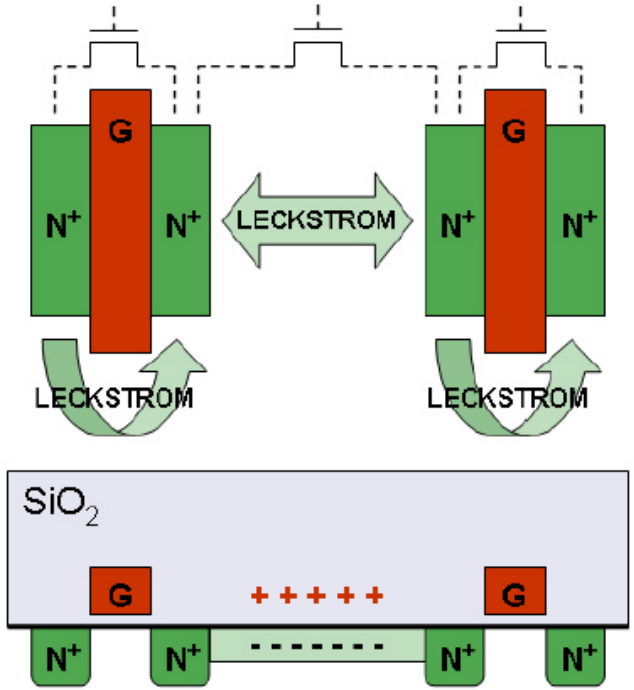
Note: Not yet clear how much rad. hardness we need for CBM... This little work is just a contribution to discussions...



Radiation Damage – very superficial

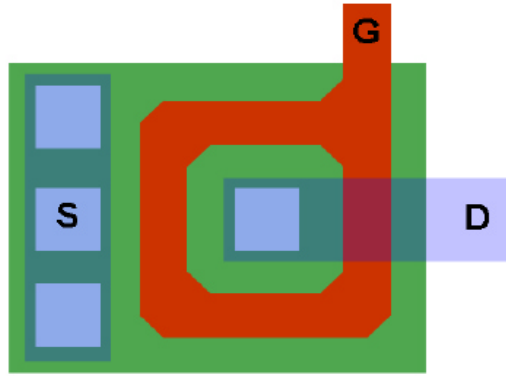
- Ionizing radiation leads to positive charges in thick oxides
  - ⇒ Threshold voltage shift – decreasing for NMOS
  - ⇒ leakage 'around' NMOS
  - ⇒ creation of parasitic NMOS (field oxide)
  - PMOS remains unaffected.

- Large local charge deposition can lead to
  - SET: single event transient = spike on signal
  - SEU: single event upset = bit flip
  - SEGR: single event gate rupture (really?)

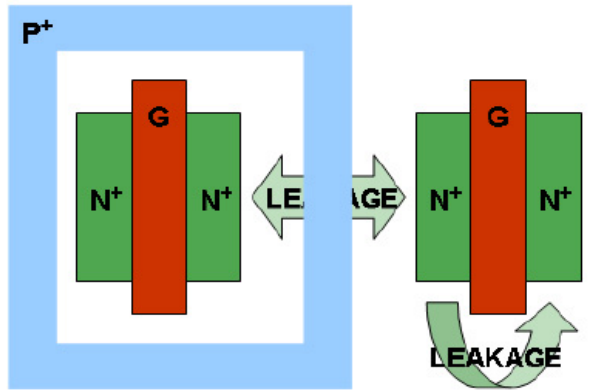


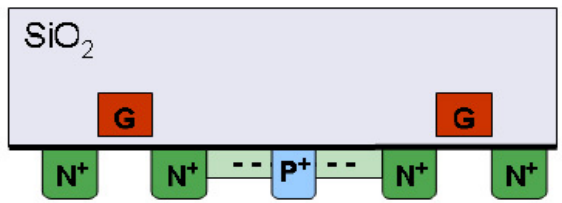
Remedies

- Enclosed NMOS (other shapes are possible!)
- Guard rings between NMOS with drains on different potential
- Special FF design / redundancy / voting / hamming... for SEU / SET



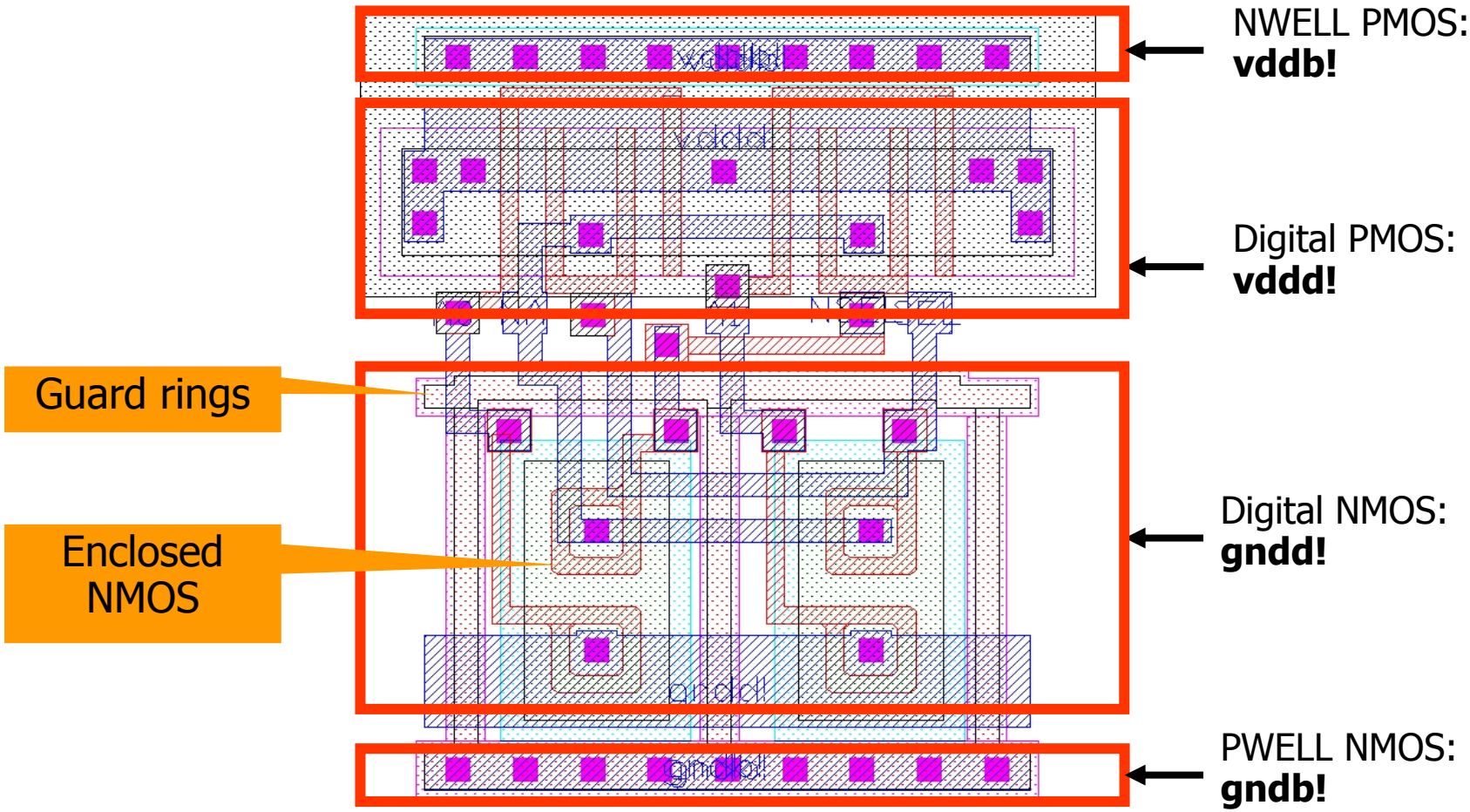
- Consequences:
  - need special extraction files
  - larger area (x4 for digital designs)
  - larger caps -> often more power in digital (x4)
  - Hard to make good NMOS current source (large L no possible)
  - Hard to make good NMOS switches (very asymmetric & large caps)





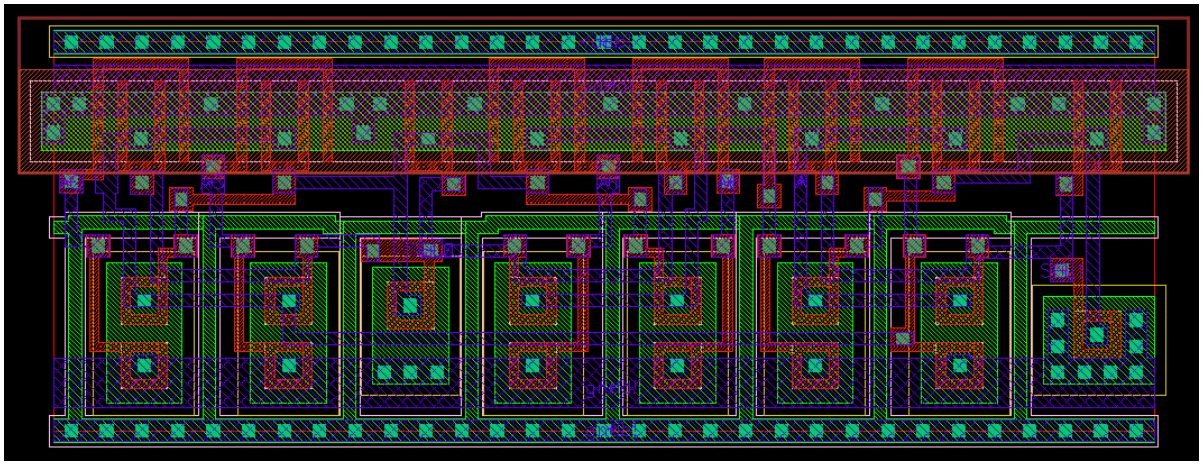
Example: radhard MUX2->1

- Our 'mixed mode' lib uses separate nets for digital wells (nwell, pwell)

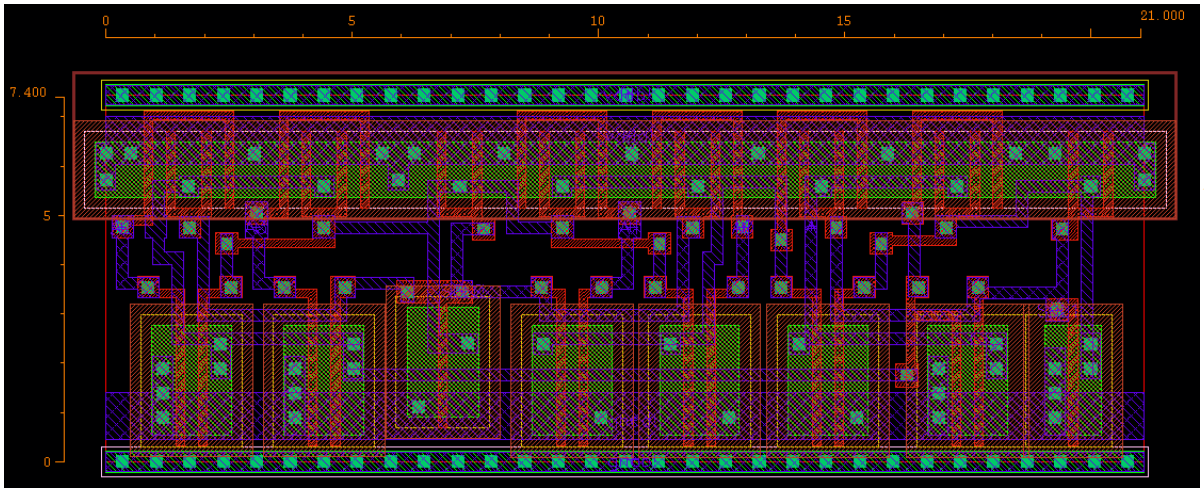


Radhard vs. Normal Layout

- We want to compare both types.
  Therefore made cells with equal transistor / layout size:



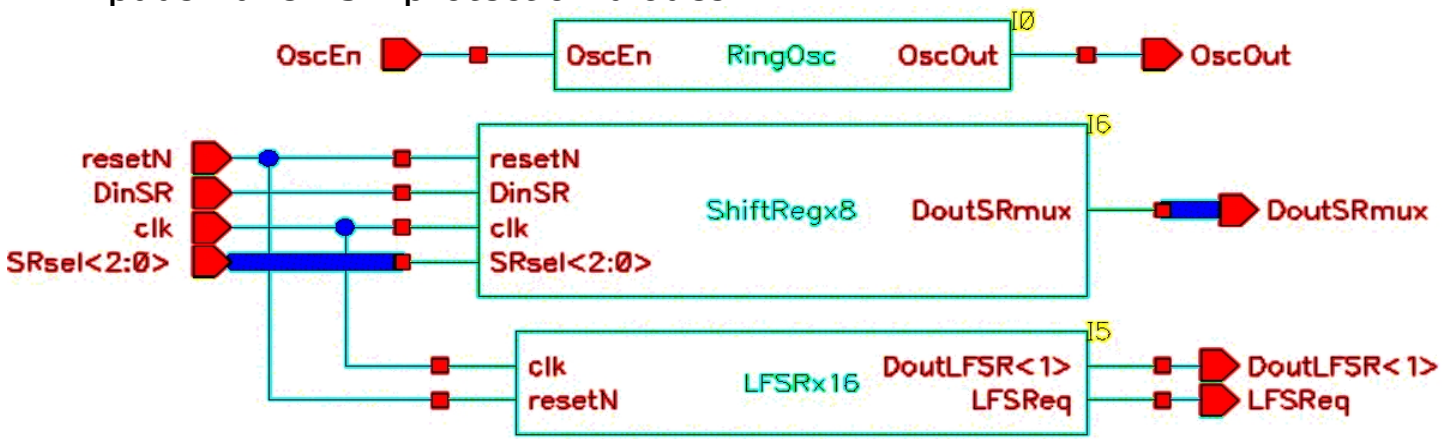
Hard



Normal

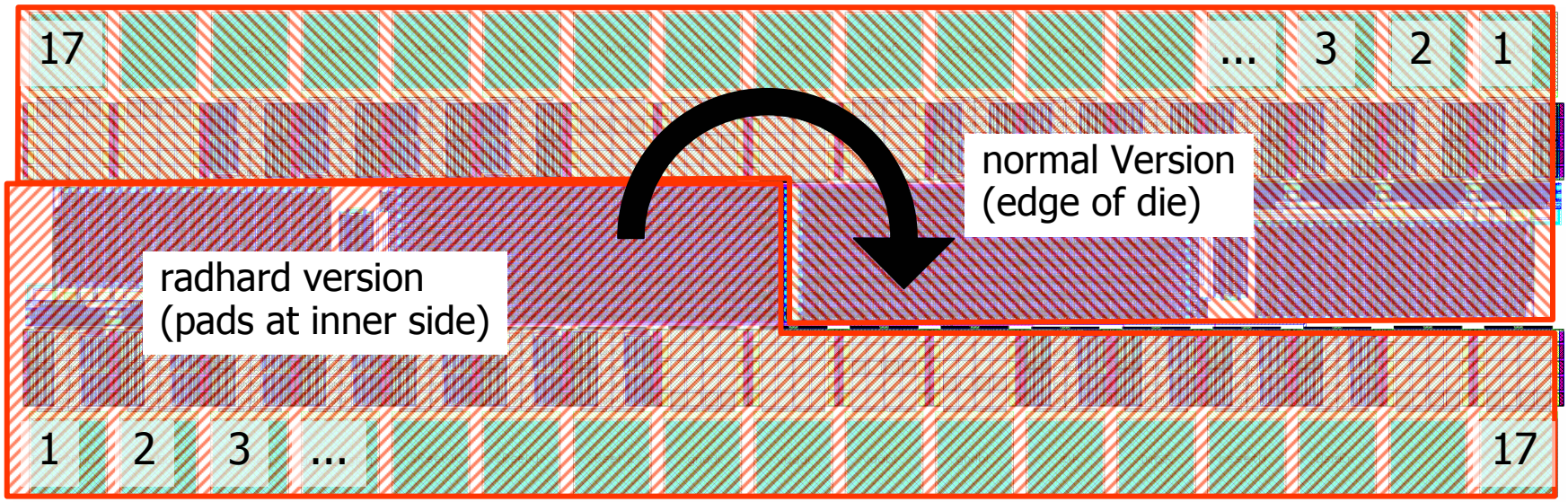
Test Chip

- Goals:
  - Verify models (speed)
  - Measure SEU during irradiation
  - Measure leakage after irradiation for 'hard' and 'non-hard' layouts
  - Keep chip very simple for easy testing with minimal equipment
- Circuits:
  - 1 ring oscillator with 101 inverters & enable. Sim. frequency: 176 MHz
  - 8 normal shift registers, 16 Bit, common data input, one output via 8-1 MUX
  - 16 linear feedback shift registers (LFSR) producing pseudo random bit sequences, 16 bit long. Test equality of all 16 LFSRs to detect SEU.
  - Rad hard output drivers.
  - All pads have ESD protection diodes

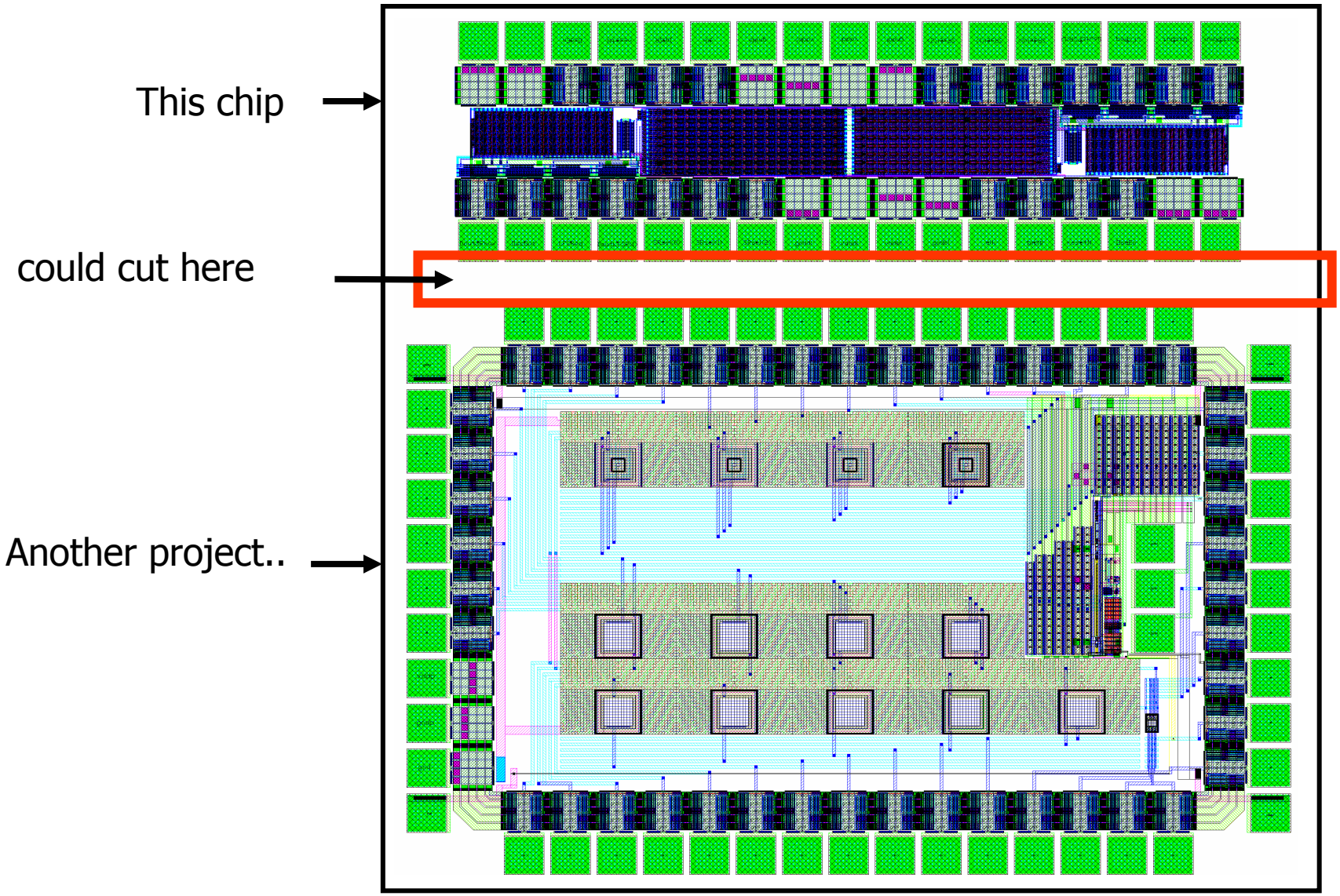


Radhard vs. Normal Layout

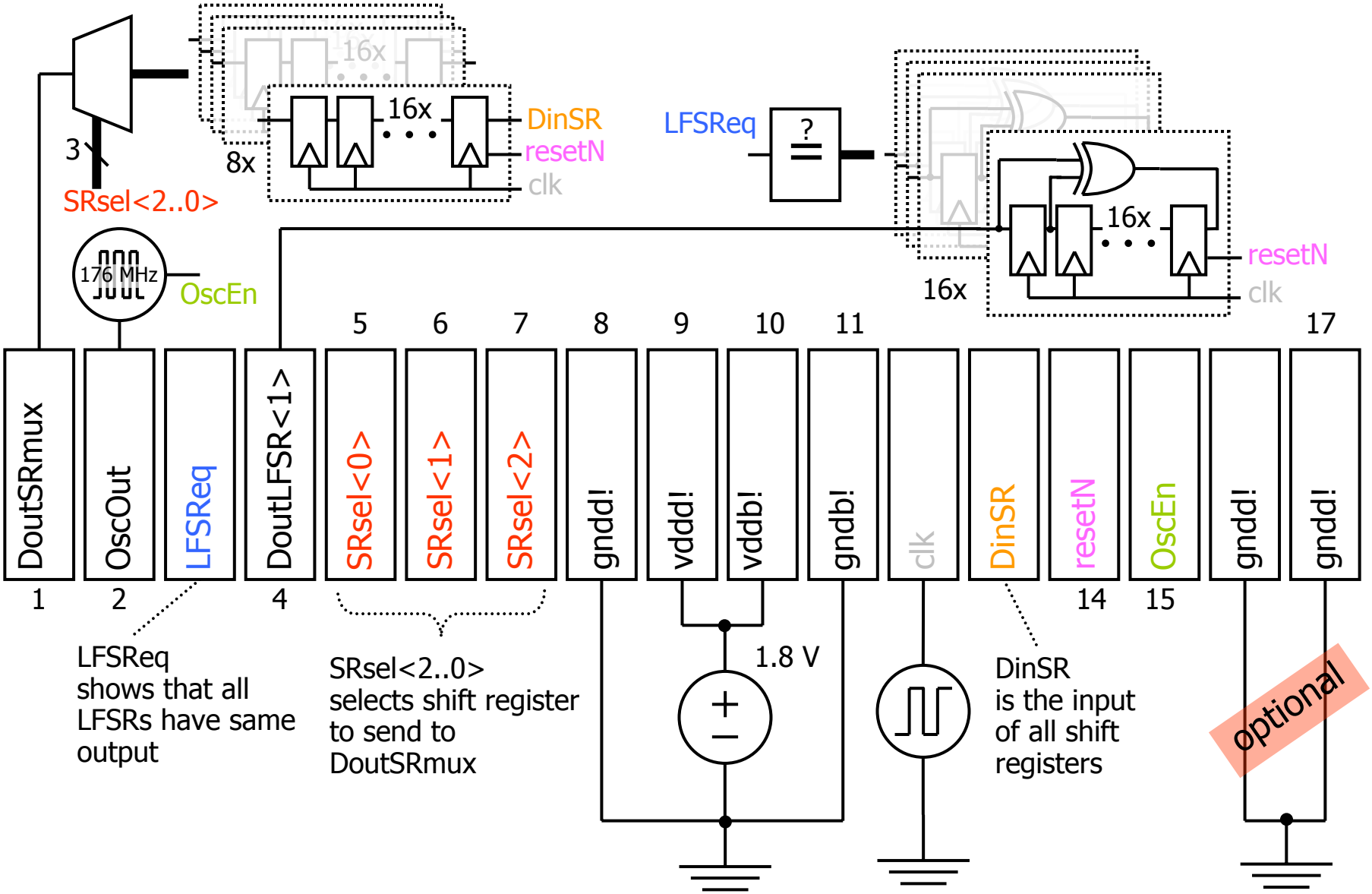
- Chip is implemented twice:
  1. radhard with round NMOS + guard rings
  2. Normal Layout. Widths of MOS are same as for round devices
- Identical pinout!
- 17 pins per side (just one side of a JLCC68)
- Switch between the two versions by rotating carrier in socket!



Test Chip Layout

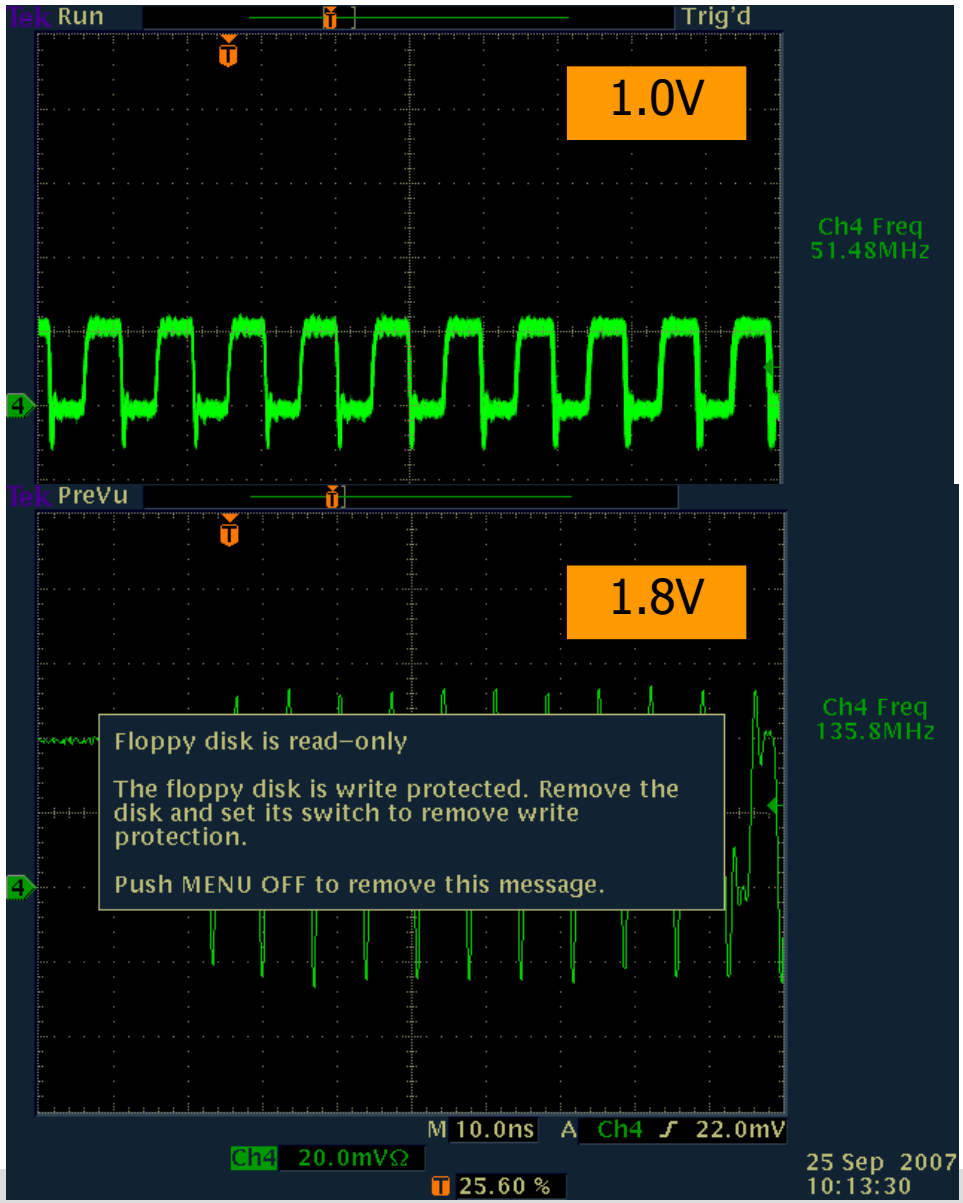


Detail of pinout…



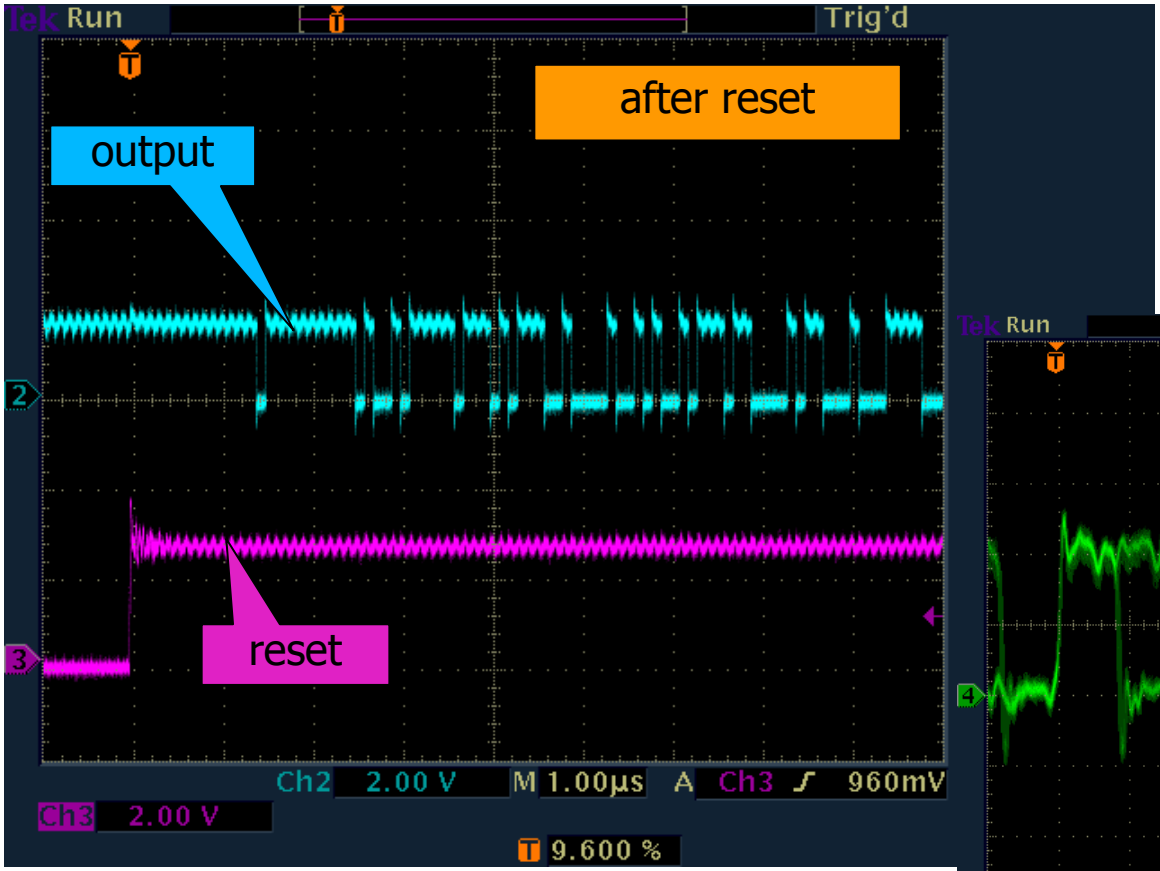
Measurements: Ring Oscillator

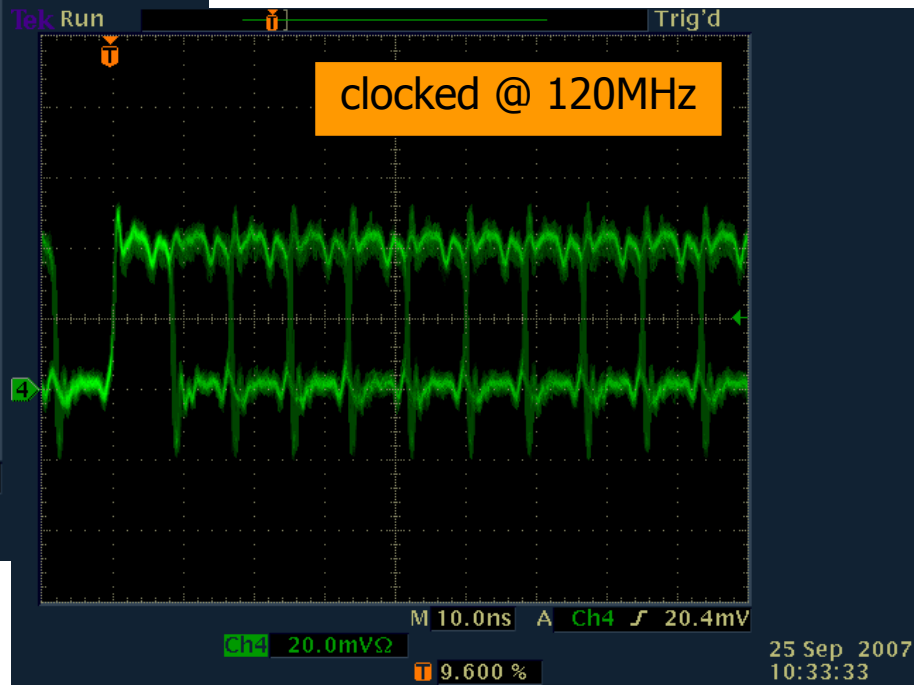
- Works as expected.
- Simulated speed: 176MHz
- Measured:
  - Supply [V] Speed [MHz]
  - 1.8 150
  - 1.7 140
  - 1.6 130
  - 1.5 117
  - 1.2 78
  - 1.0 51



Measurements: LFSR

- Works as expected
- Produces nice spectrum on Analyzer...





Problems & Summary

- Shift registers also work as expected
- Problem: Large supply current. May be setup but more likely wrong type of substrate connection somewhere...

- Good agreement in speed. Must check voltage dependence.

- Next steps:
  - Decide if irradiation of this is interesting
  - May resubmit in 3 weeks if there is a bug. May increase register length.