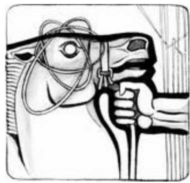
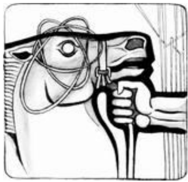

Moscow Engineering Physics Institute (State University)

Status of Radiation Tolerant Blocks for STS

A. Simakov / V. Shunkov

10 CBM Collaboration Meeting 2007 Sept. 25-28



Moscow
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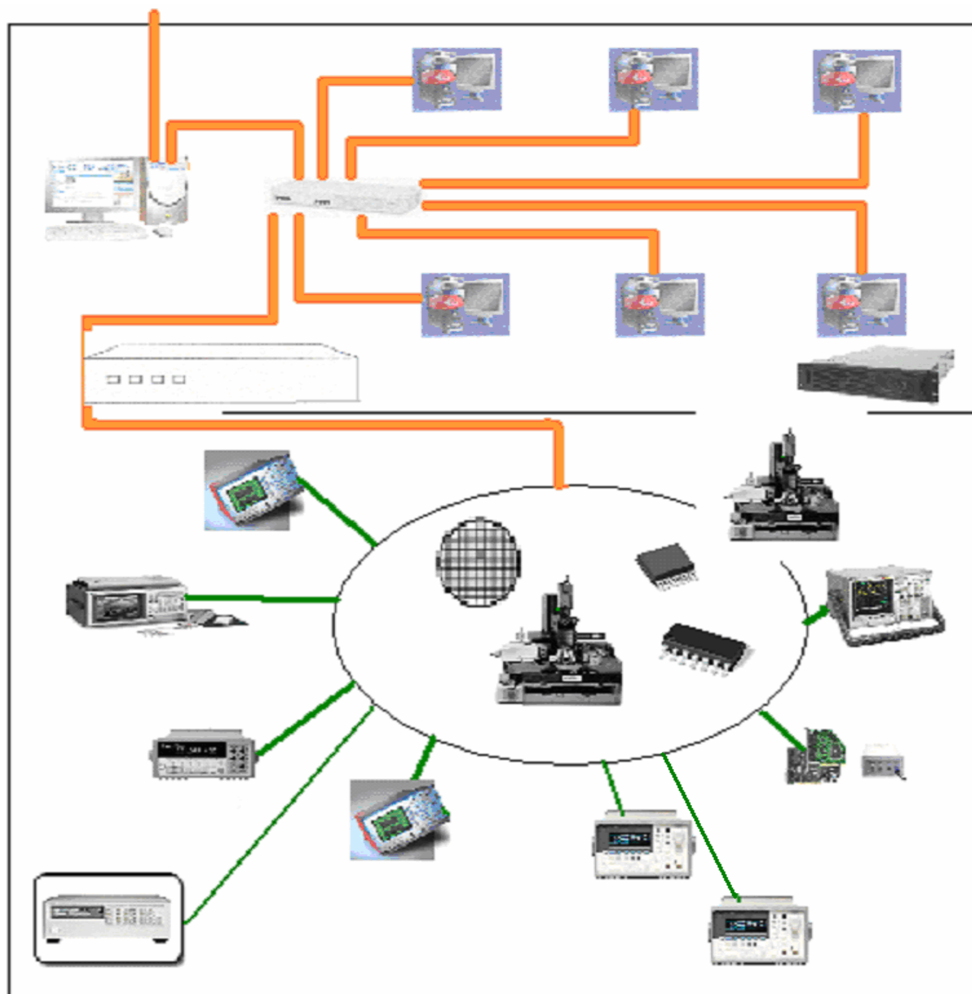
Outline

1. List of tasks to be solved
2. Development of measuring infrastructure and test software
3. Rad-hard test facilities in MEPhI
4. Some views on rad-hard design of IP blocks

The problems
(from Christian Schmidt's TOPlan)

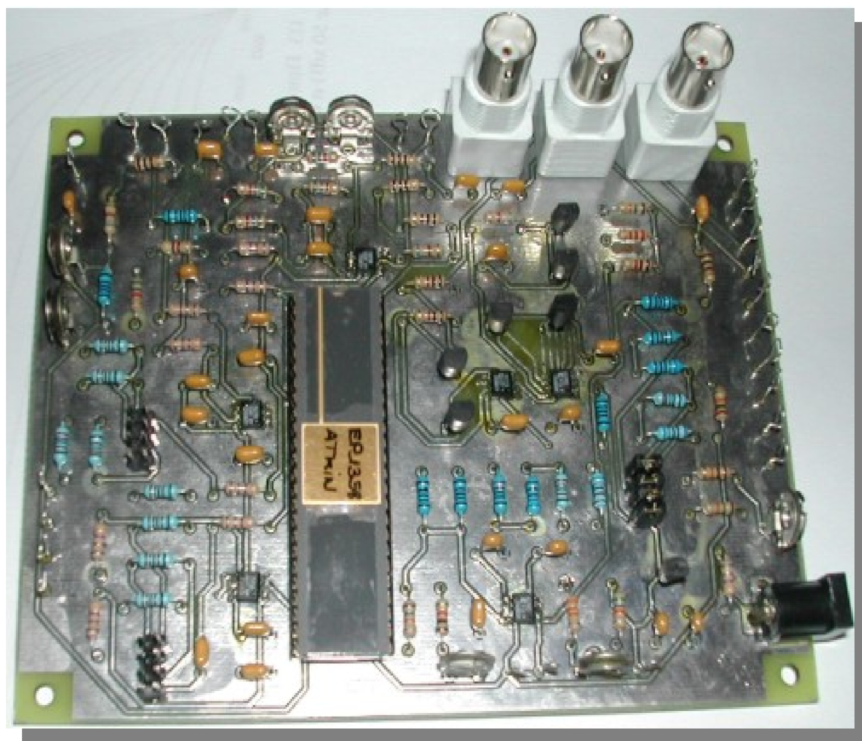
1) Minimum setup for total dose effect measurements:
Need to apply at least clock and bias during the test
2) Design and Submission of Test circuits
3) Development of testing software
4) Design of rad – hard IP-blocks
5) New rad-hard tests facilities
6) SEU Error Correction
7) Radiation Hardness Tests

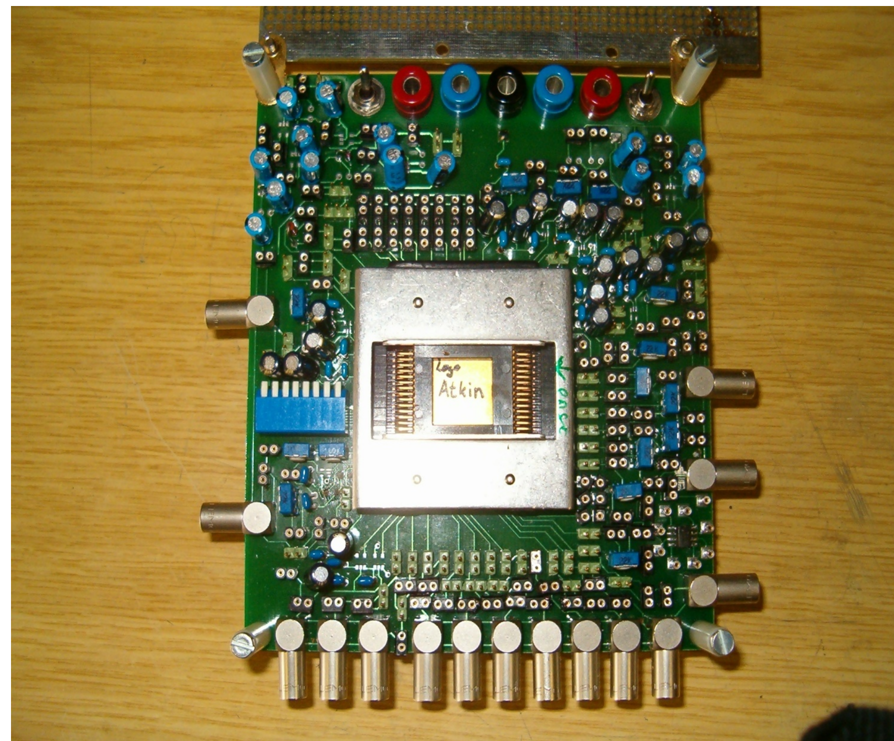
New Computer Aided Measuring Center



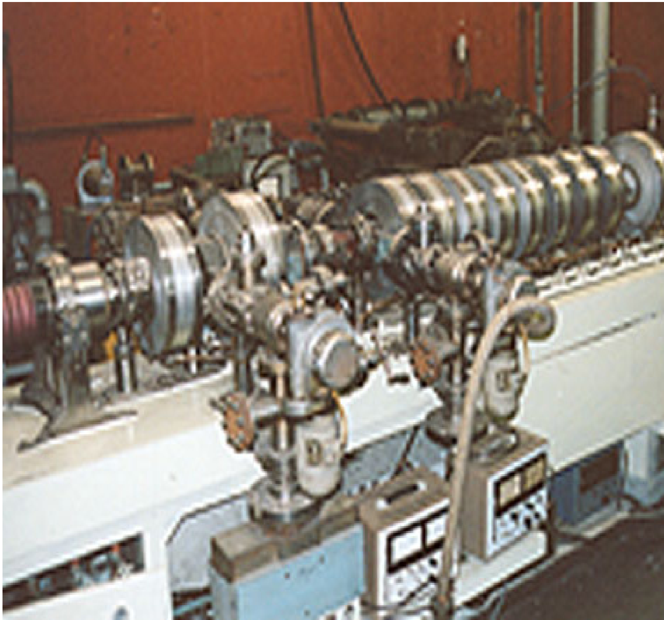
- Center are equipped with automatic Agilent devices and Sun computer cluster
- Mentor Graphics has supplied a TEST COMPRESS software
- Sponsorship is from Rosobrnauka and Rosprom

Examples of Test circuits





MEPHI's Accelerating Center
Linear Electron Accelerator U-28



- Particle energy - 8 MeV.
- Max.beam current – 300μA.
- Dose rate (at I~10^{10}e/cm^2.s) – 1x10^2rad/s.
- For D=10^6 rad. Exposition time- 10^4 s, (~3h).
- Dose rate at γ-conversion (1m) – 10 rad/s.

New rad-hard tests facility
Linear Proton Accelerator

- E_p – 1 ÷ 3 MeV
- T_{pulse} – 1 ÷ 100 µs
- I_{pulse} – 1 mA
- $Square_{pulse}$ – 5 ÷ 8mm
- T_{pulse} – 0.1 ÷ 50 s

Some views on rad-hard design of IP blocks

- Three approaches for extreme radiation hardness achieving
- Single Event Effect hardened logic
- SOI dose and SEE hardened test chip

Three rad-hard achieving approaches

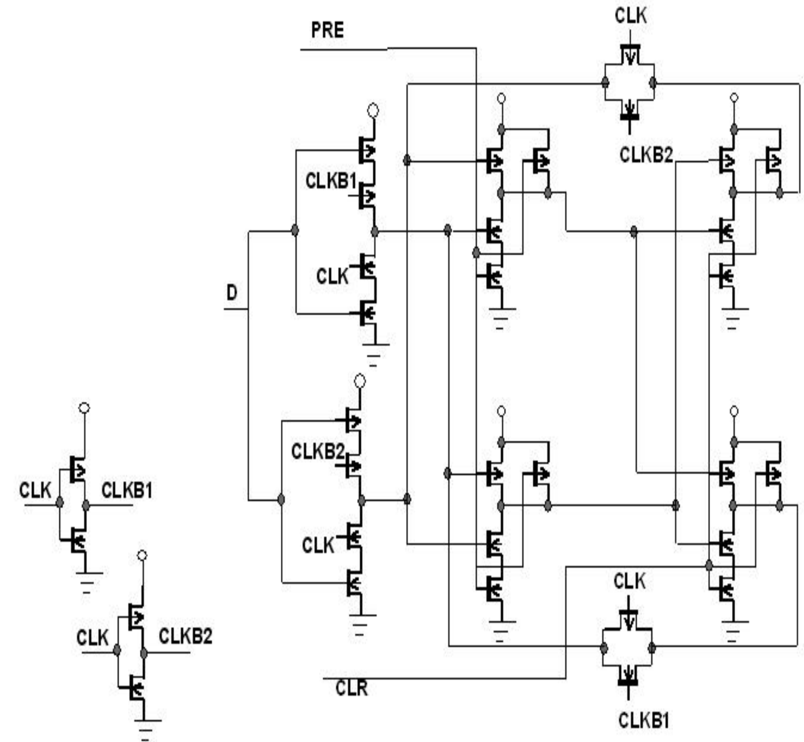
- CBM electronics should be extremely radiation hardened versus Total Ionizing Dose and Single Event Effects
- Standard technologies and circuits could not provide this requirements

Three main approaches in rad-hard achieving are:

1. Special radiation hardened technology (e.g. SOI)
2. Circuit and layout design methods on standard technology
3. Combination of technology and design hardening

Single Event Effect Hardening

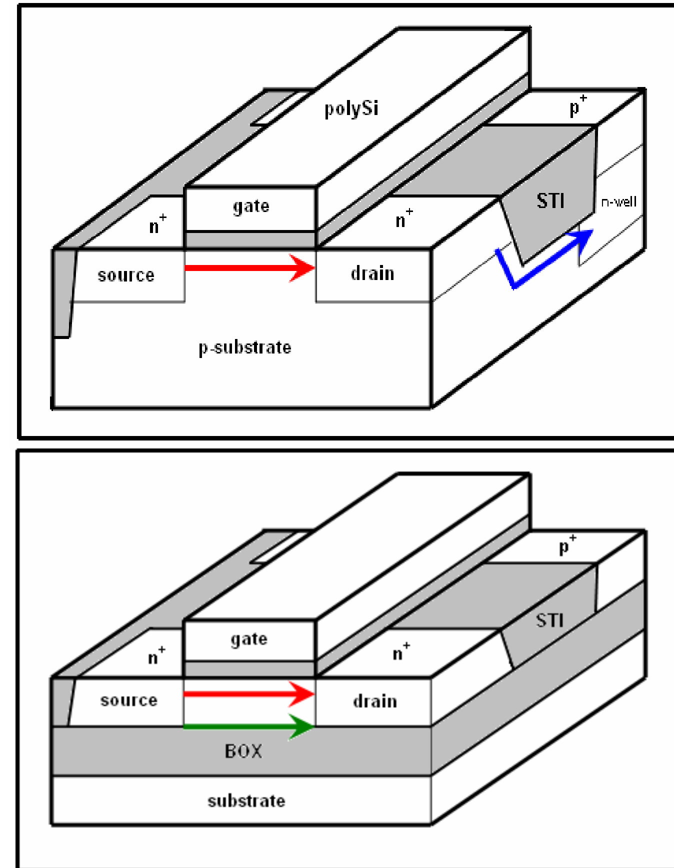
- SEE can be suppressed by circuit methods like triple-mode redundancy
- The cost is triple power and area
- Another method is to use SEE-hardened primitive cells with internal redundancy



D trigger with internal redundancy

Test Chip

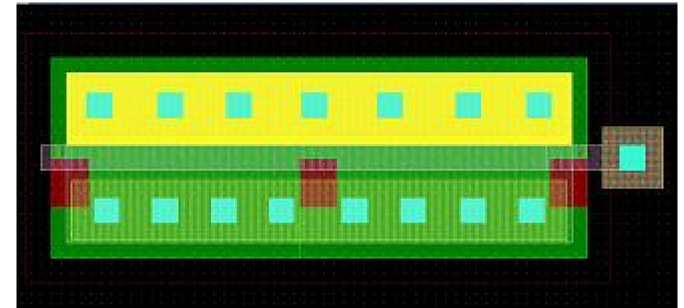
- Test chip has been made on SOI 0.5µm on 1x1 SRISS* RAS fab in Moscow
- Hardened circuits demonstrated **9.6 Mrad** dose tolerance vs **50 krad** of standard circuits
- Single Event Rate in SOI was in order of magnitude smaller than 0.5 µm bulk and similar to 0.18 µm bulk
- **Strip** transistors with extreme TID and SEE hardness has been designed

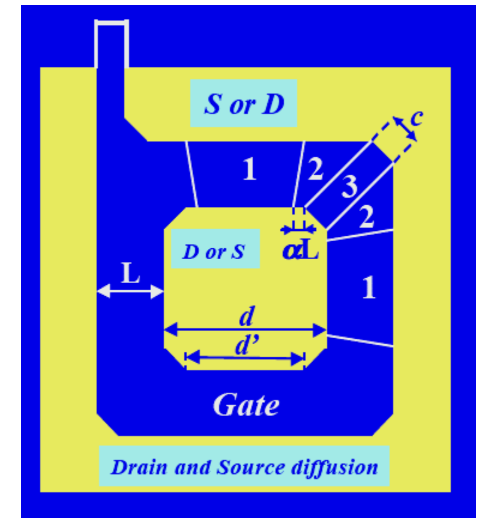


* - Science Research Institute for System Studies

SOI rad-hardened strip transistors

- Bulk ELT may be designed with **W/L > 7** that leads to increasing power consumption and area
- SOI strip transistors with same hardness may be designed with **W/L = 1.4**
- **SOI allows area and power consumption reduction for radiation hardened circuits**





Thus…

Rad-hard design in MEPhI

- SEE-hardened logic circuits has been designed in 1x1 SOI 0.5μm and UMC bulk 0.18 μm
- SOI test circuits demonstrated high dose and SEE hardness
- UMC tests have been designed but still not fabricated
- Designed SEE-hardened circuits can be implemented in CBM control logic

1x1fab SOI advantages

- Known **9.6 Mrad** dose tolerance
- No latchup
- Good SEE tolerance
- Full-custom ASICs can be fabricated in very small series
- High interest of SRISS RAS in collaborating in CBM