Status of Derandomizer electronics

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Outline

- Status of the de-randomizer electronics development
- Progress on chip design and plans

De-randomizer

(remake of the old slide of 2005)

Analog derandomizer is a unit performing neuron-like processing, but in an analog field.

It is a deadtime free analog unit with n-inputs and m-outputs, $n>m$.

Thus it allows to reduce the number of following ADCs.

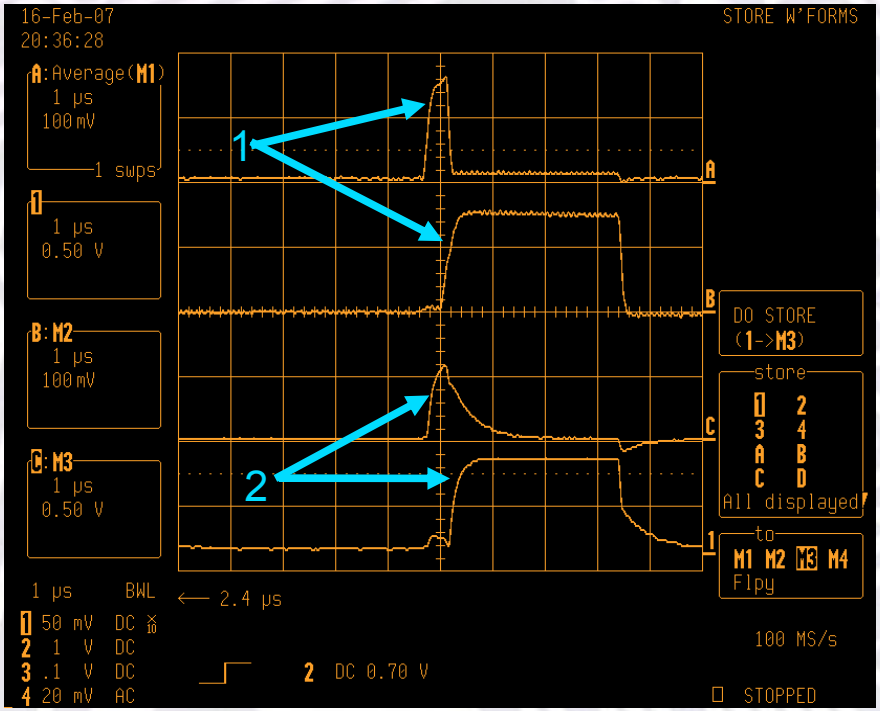
The derandomization procedure implies the skipping of empty channels and thus is indivisibly bound with data sparcification.

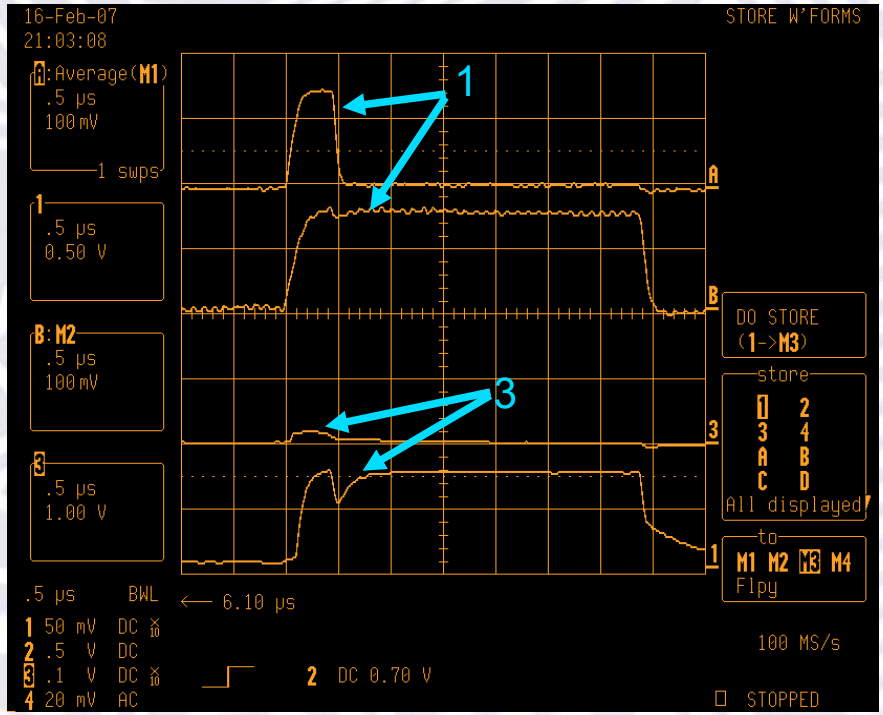
Efficient processing of the randomly appearing signals by blocks, having a dead time, needs the choice of a proper architecture.

Status

- 4→2 derandomiser prototype in UMC 0.18 um showed functionality
- 128→16 one is under development

Crosspoint switch





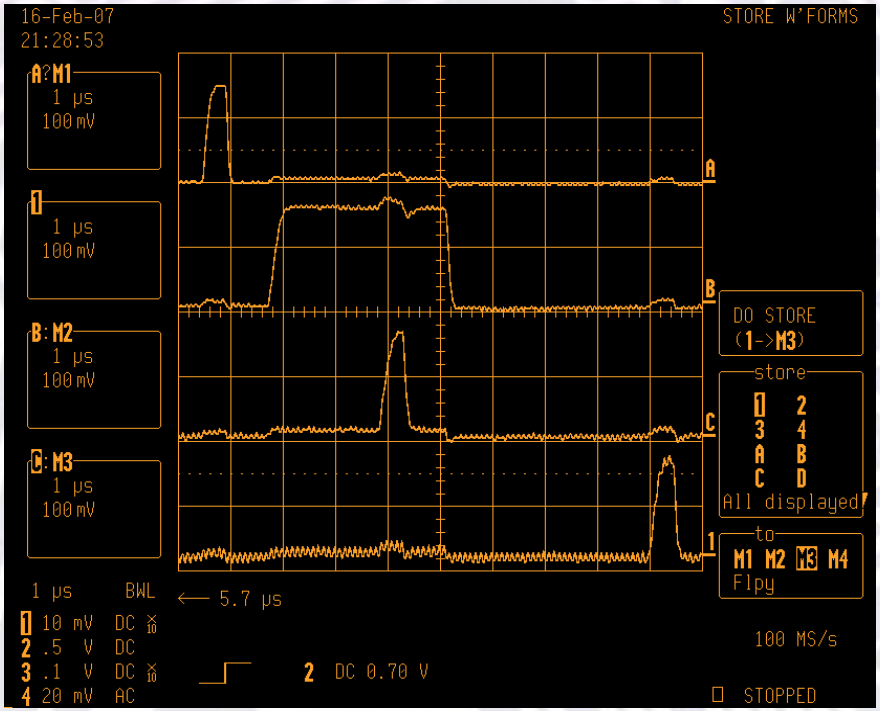
Small delay between two signals
(partially overlapped)

Two signals at the same time
(full overlapping)

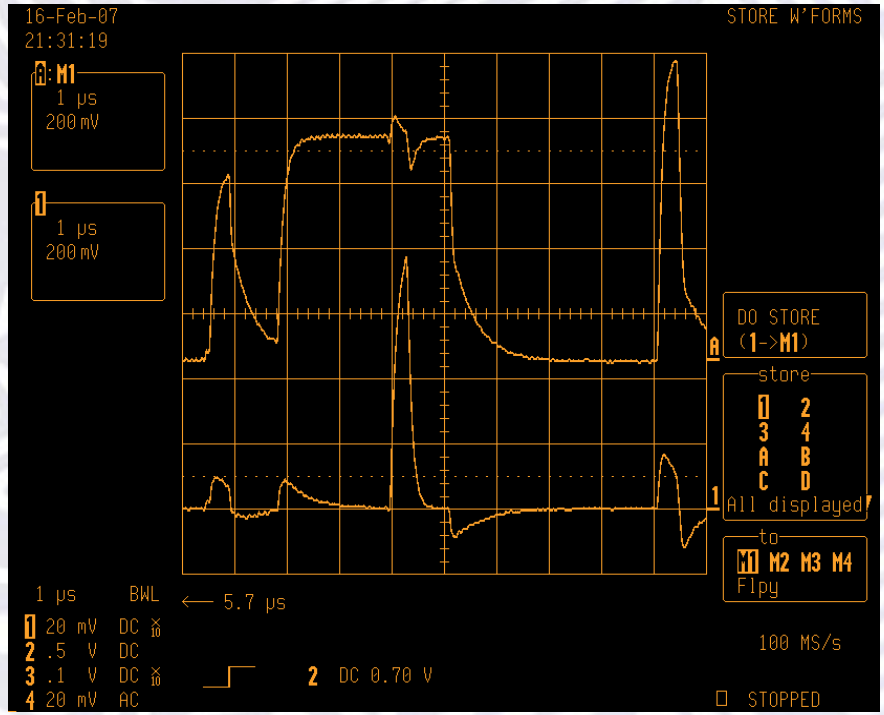
- 1-comparators
- 2-inputs
- 3-outputs

4 --> 2 prototype

Crosspoint switch



4 signals (comparator outputs)



2 crosspoint switch outputs (after amplification)

4 --> 2 prototype

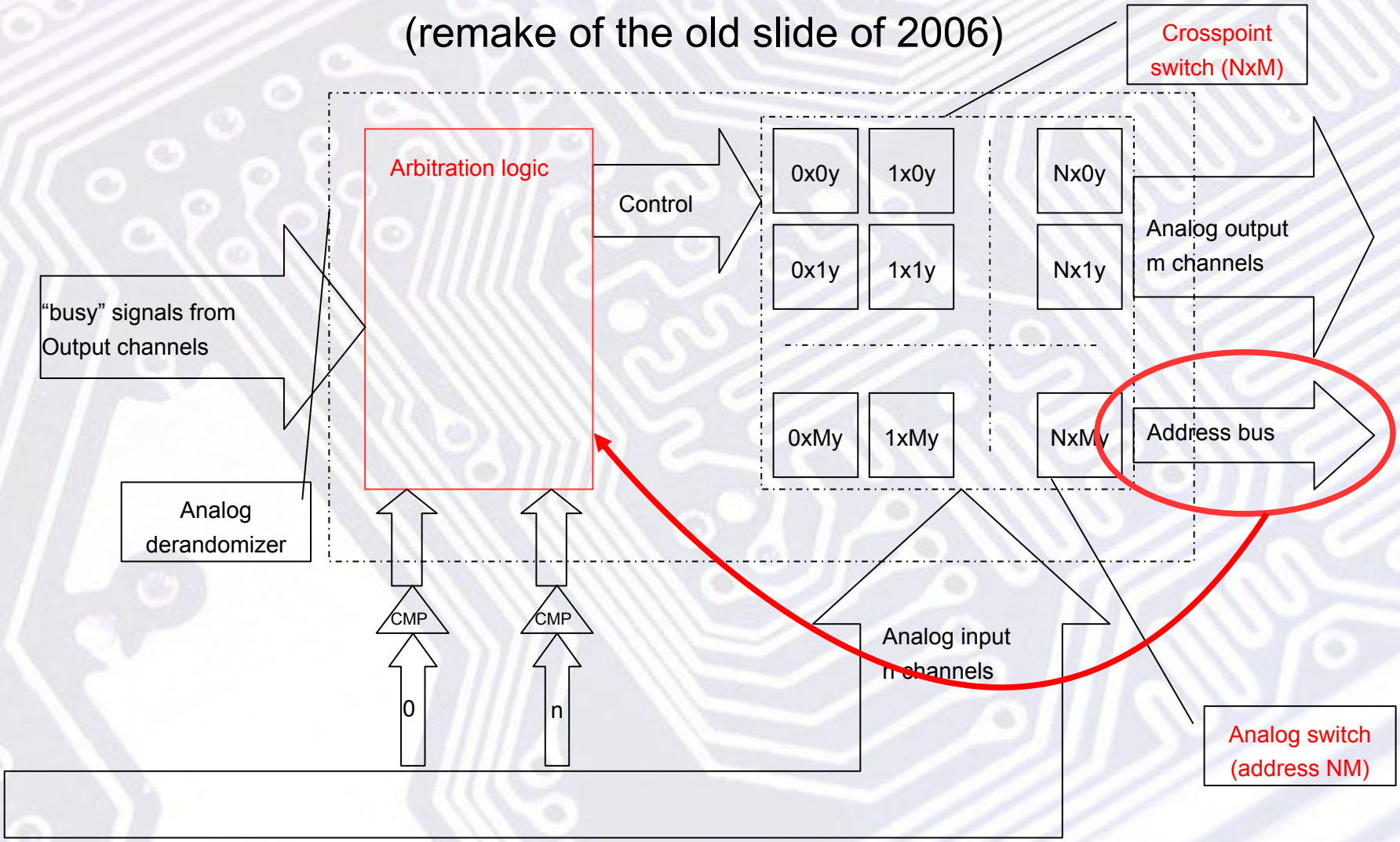
Development of the de-randomizer 128→16

A. Klyuev(PhD student), M. Trubetskoy(diploma student)

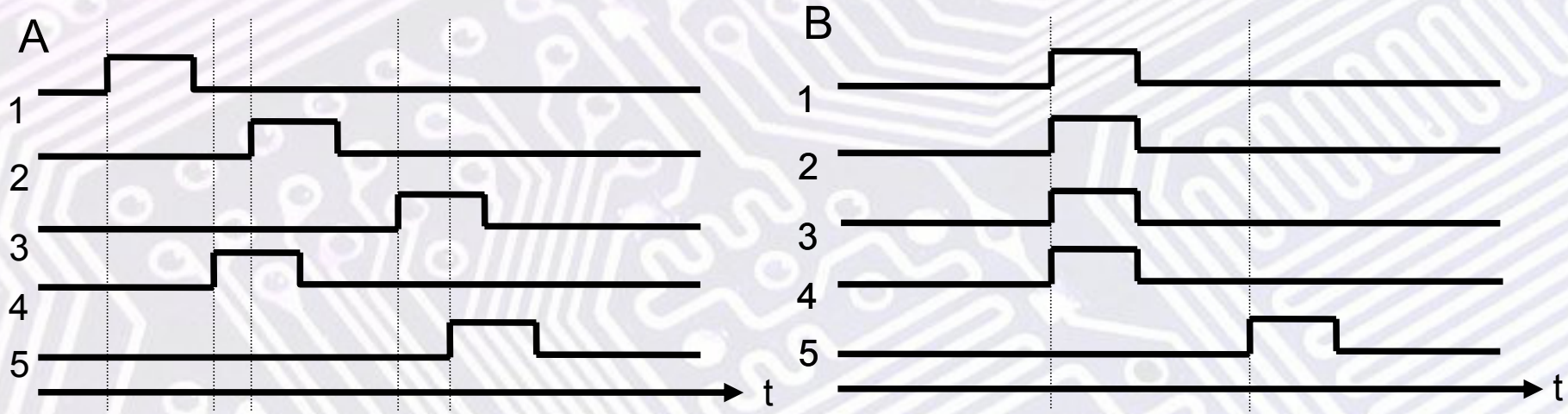
CBM Collaboration meeting (September 25 - 28, 2007) @ FZD, Dresden

Structure of analog de-randomizer

(remake of the old slide of 2006)



Two types of considered working conditions



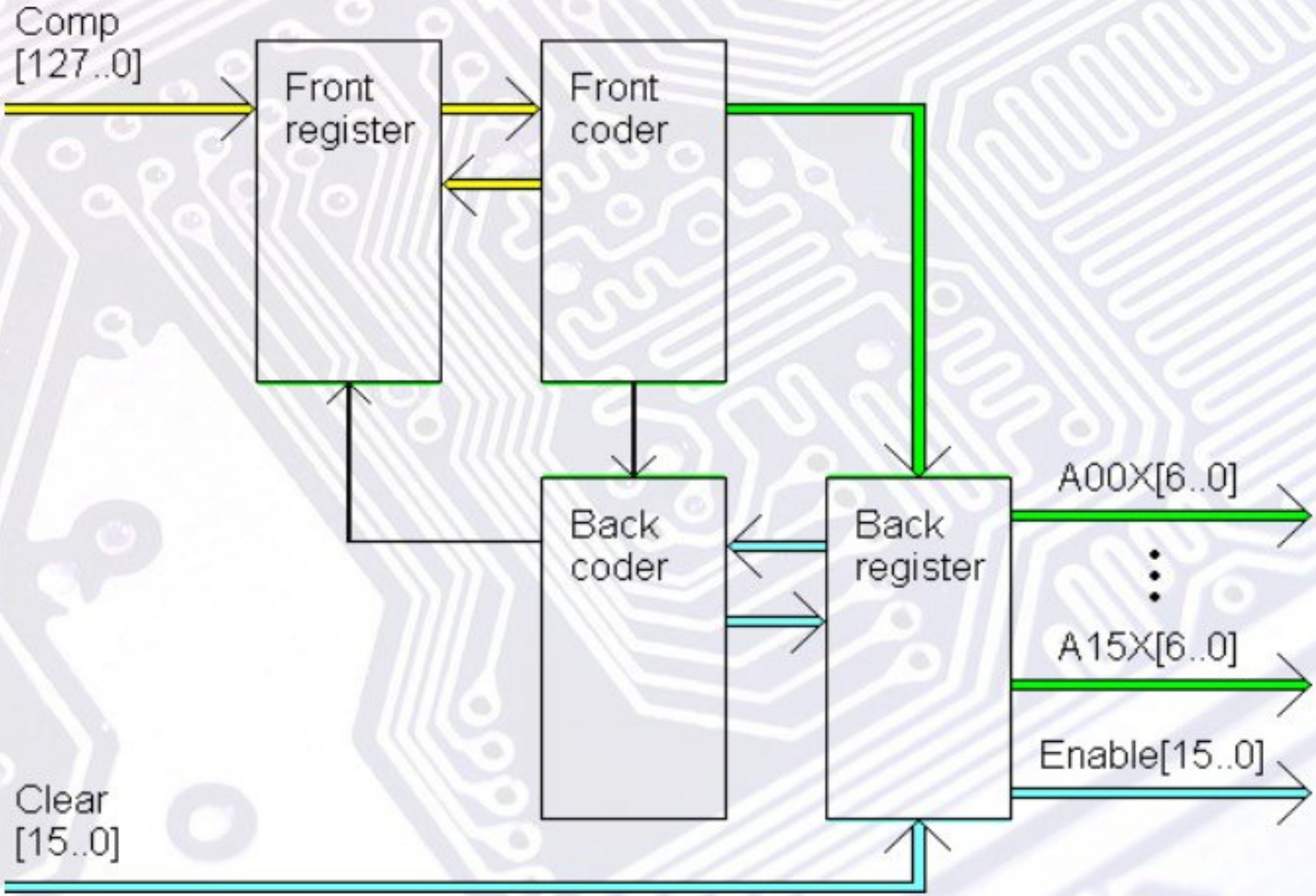
The choice of de-randomization factor (d) strongly depends on working conditions of the system. Let's consider 2 types of working conditions:

A. The most probable event – pulses occur NOT simultaneously, uniformly in all channels and have equal duration. The 1st prototype is based on this variant. The FSM for this case exists and can be scaled to other d (128->16, 64->40, 59->19, etc. It is better when the number of the channels is divisible by 2 however).

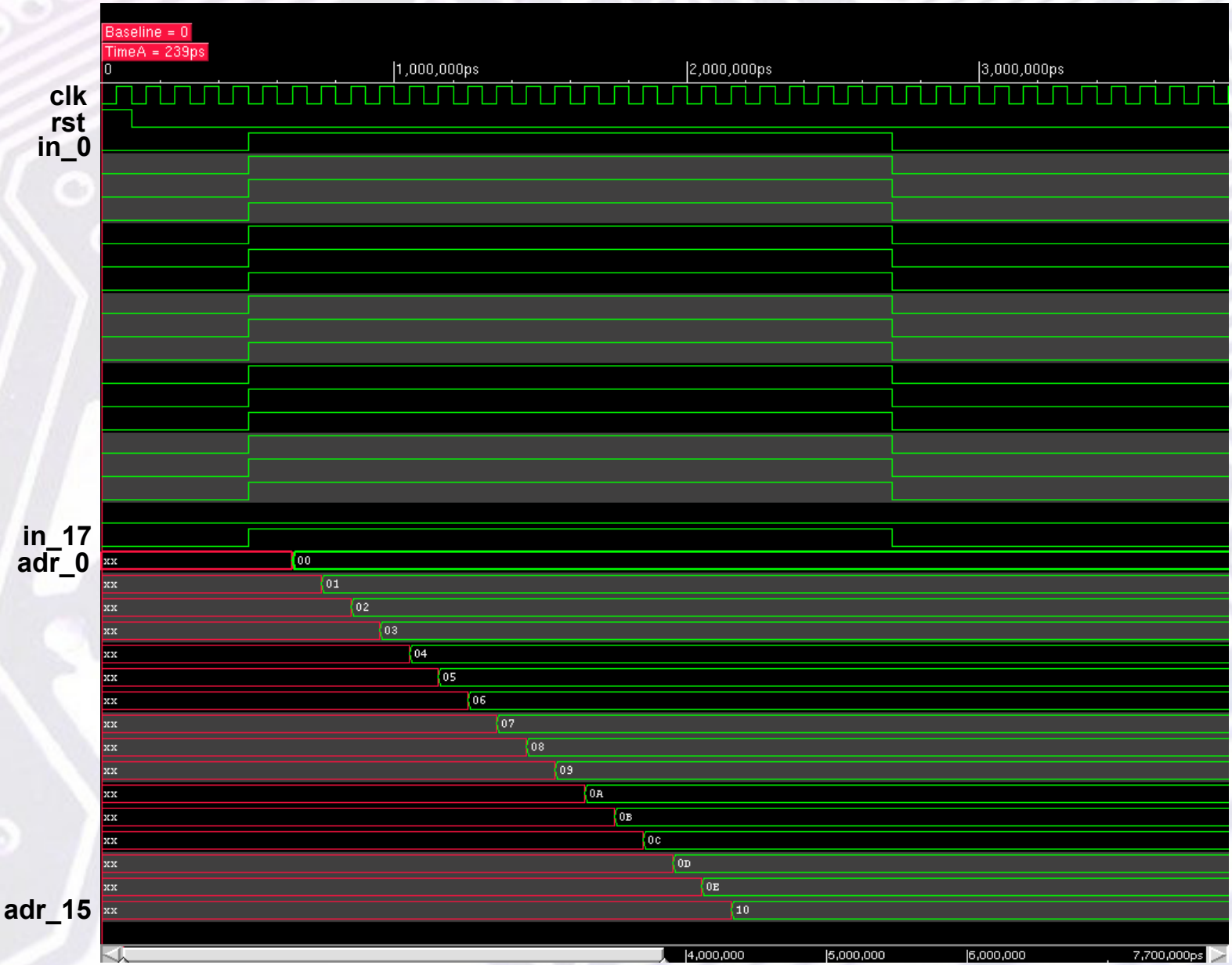
B. The most probable event – many pulses occur simultaneously ($T>>\Delta t$). It is really typical for the detectors, taking into consideration the cluster nature of their pulses. For this case we have to modernize the existing FSM, so it will be able to commutate one channel per clock.

1->1
2->2
3->4(3rd output channel occupied at this time)
4->5
5->6
Etc.

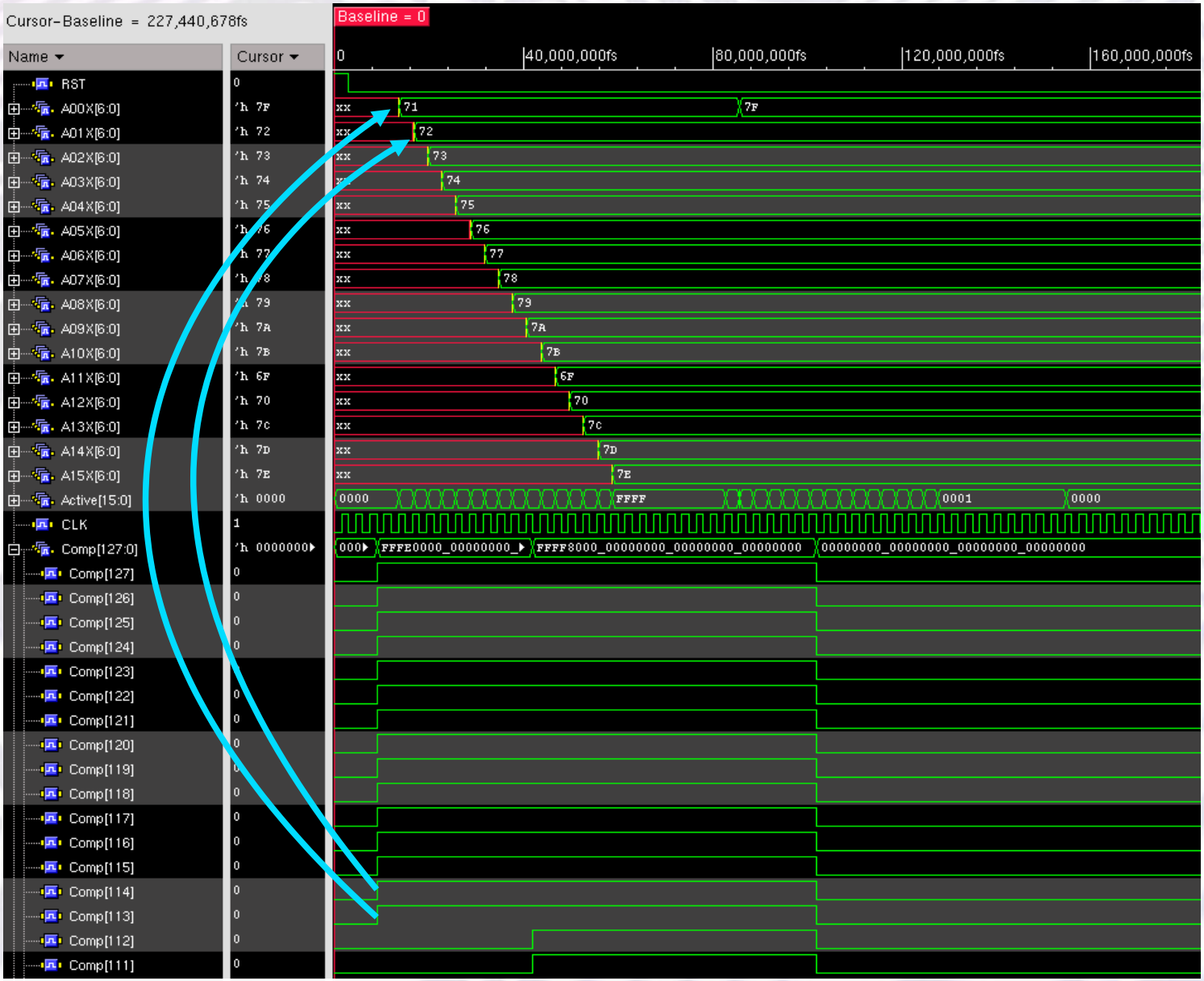
Structure of new arbitration logic



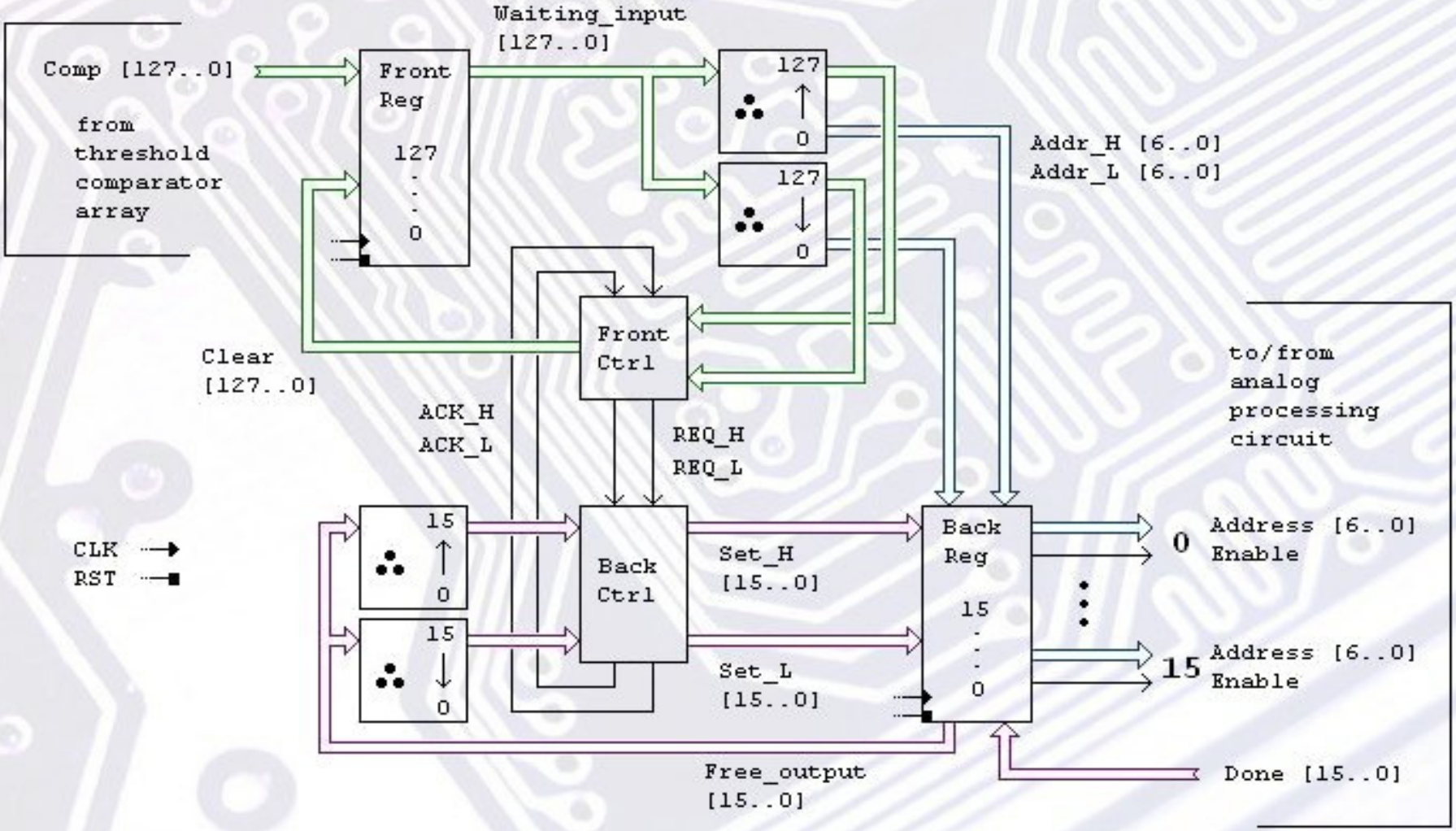
Simulation of arbitration logic (RTL model)



Simulation of arbitration logic (synthesized netlist for UMC 0.18)



Structure of the last variant of arbitration logic



Simulation of the last variant arbitration logic (synthesized)

Progress on chip design

Main tasks since previous meeting:

- Familirization with the N-XYTER (Simulations of critical blocks) (is under study by 2 diploma students). The test results of N-XYTER would be useful.
- Development of a new release of derandomiser electronics (128 → 16 structure) (talk of A.Kluev)
- Study aspects of improvements of radiation hardness (talk of A.Simakov/V.Shunkov)
- Development of low power rad-tolerant ADC (talk of A.Gumeniuk)

Plans

We would like to:

- Develop the following building blocks and participa with them in the UMC 0.18 um MPW run for:

the CBM-XYTER:

1)ADC

2) front-end block

the back-up solution:

3)128→16 derandomiser

4)some rad-hard test structures

- Improve facilities for:

chip design and measuring

rad-hard tests