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Pipelined ADC

We propose two variants:
low power and **reliability optimized**

Proposed designs

We plan to test



- 7 bit **28** mW 20 Msps
reliability optimized ADC



- 9 bit **9** mW 20 Msps
power optimized ADC

ADCs features



reliable



low power

- **Doubled** number of S/H circuits
- OpAmps and comparators are **shared** between adjacent stages

ADCs features (cont - 1)



reliable



low power

- Using only **accurate** and offset **compensated** comparators
- Using **zero** DC consumption dynamic comparators

ADCs features (cont - 2)



reliable

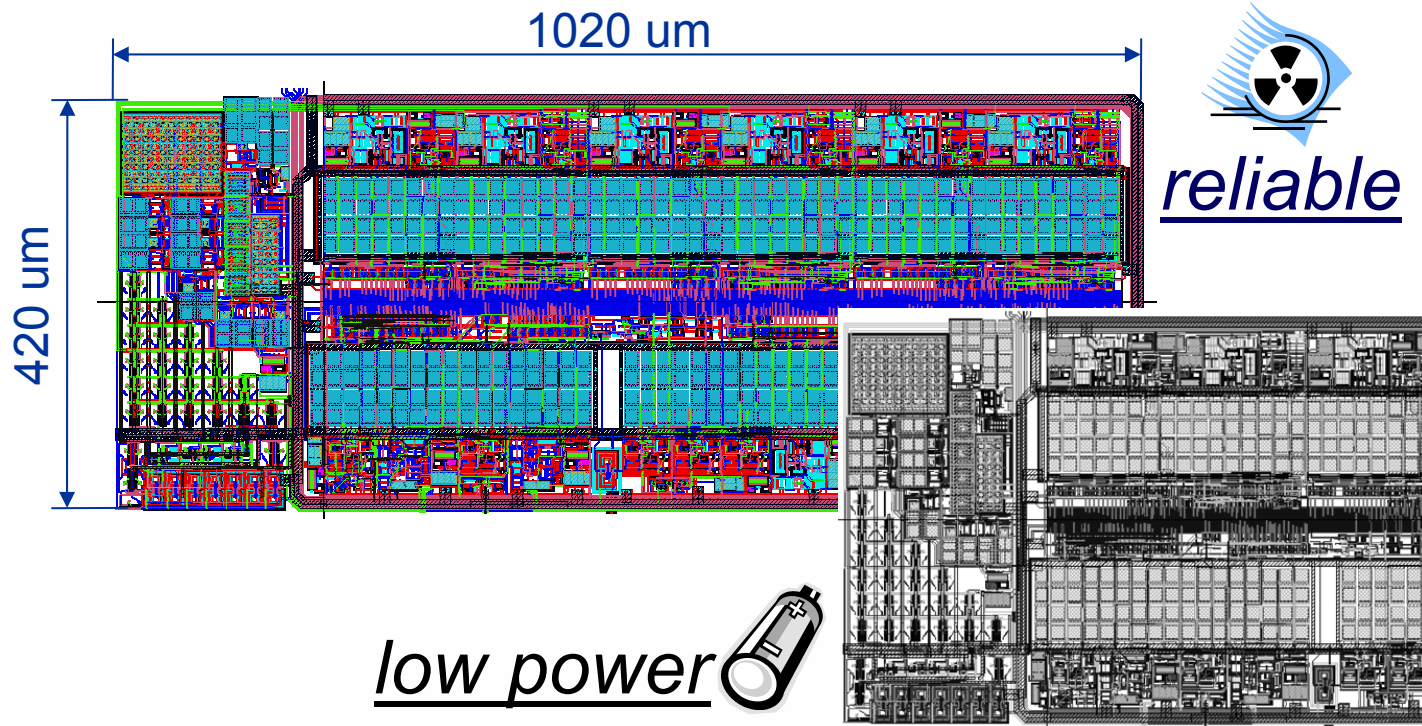


low power

- Using **maximum** capacitor values and opamp currents for tolerable power
- Capacitor and opamp current values are **scaled** along down the pipeline

ADC area comparison

The low power ADC has a **halved** area comparable with reliable variant



Reliability vs. low power



reliable

- Higher degree of accuracy
- Functional redundancy
- No dynamic circuits – only relatively high static current comparators



low power

- Lower power consumption more than 2 times
- Higher resolution
- Lower area
- Lower conversion latency – 6 cycles instead 8

Conclusion

We going to examine two ADC design with



• Resolution	7	9	bits
• Sampling Rate	20	20	Msp/s
• Power consumption	28	9	mW
• Input capacitance	1	0.7	pF
• Supply voltage	1.8	1.8	V
• Process	0.18um MM/RF UMC CMOS		
• Feature	reliability	low power	