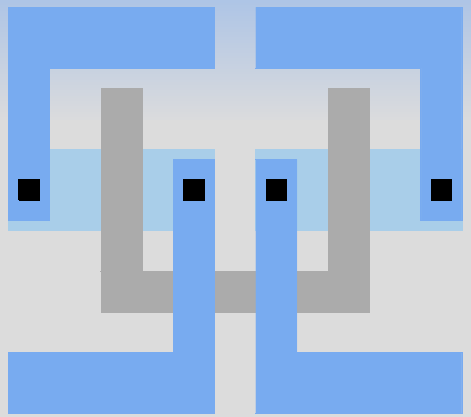
CBM-XYTER design aspects



Schaltungstechnik
und Simulation

Tim Armbruster

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10. CBM Collaboration Meeting

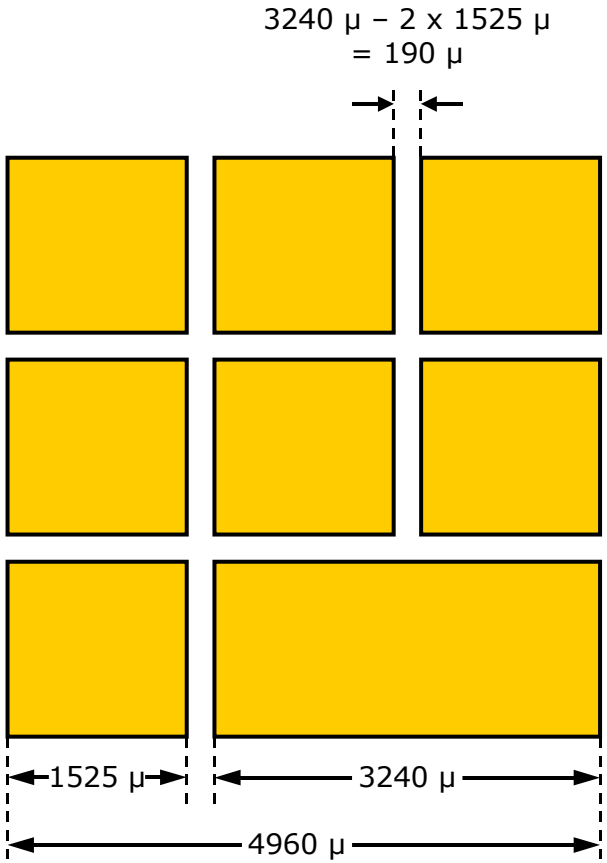
in Dresden

25.09.2007 - 28.09.2007

Chip Geometry

Reminder: UMC018 - Possible Chip Dimensions

- Submissions via Europractice:
  - Full 5 x 5 mm^2 runs every 2 month, 14.5k€
  - MiniASIC with blocks of $(1.525mm)^2$ every 4 months, 2.4k€ per block
  - ~2.5 months delivery
  - Cost break even at 6 MiniASIC Blocks !
  - Note: In MPW runs chips may be larger due to cutting!



Strip R/O: General Geometric Relations

basic relation:

chip_pitch

= chip_size + gap

= 2 * (pad_length + edge)

+ N * channel_pitch

+ gap

considering strip pitch:

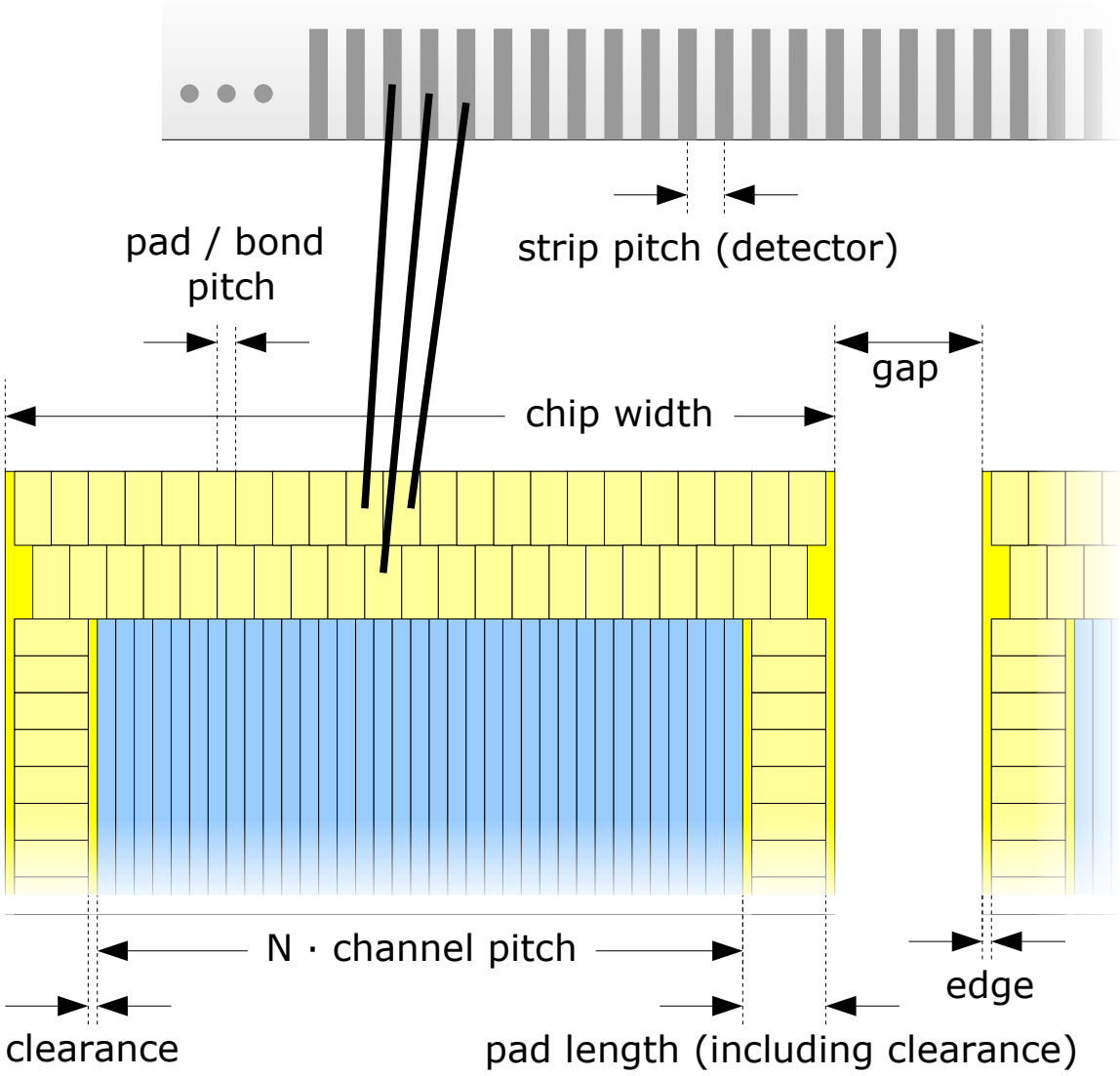
strip_pitch

≥ (chip_pitch) / N

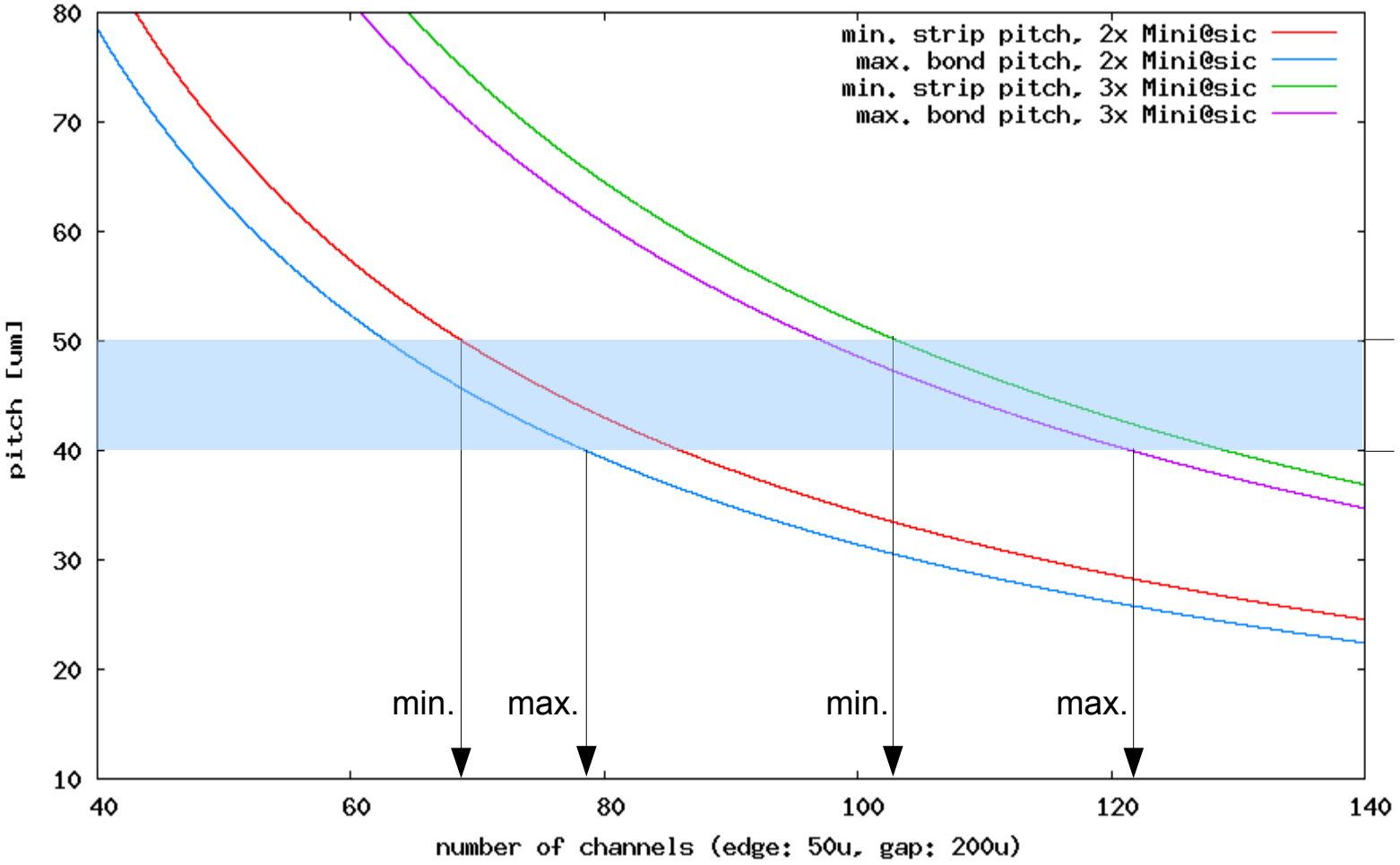
considering bond pitch (every channel needs one analog input pad):

bond_pitch

≤ (chip_width – 2* edge) / N



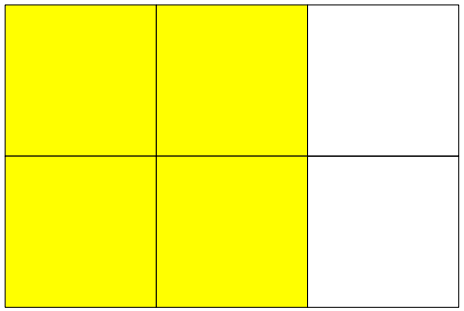
Number of channels



=> Poss. num of channels (50u strip pitch, 40u bond pitch): 2x Mini@sic: 68 – 78, 3x Mini@sic: 102 - 121

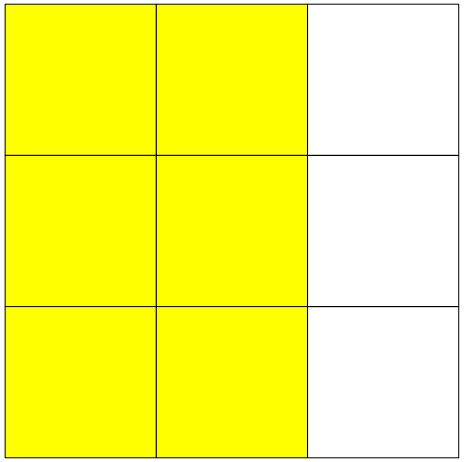
Realistic Chip Sizes

- Note: Chip size aspect ratio limited to 2:1!
- Some realistic chip dimensions (@ pad length150u, edge 50u, gap 200u, **bond pitch 40u, strip pitch 50u**):



Option 1:

- 2x2 or 2x3 Mini@sics
- 68 – 78 channels
- channel pitch: 42um - 36um
- channel length: ~2,7mm or 4,4mm

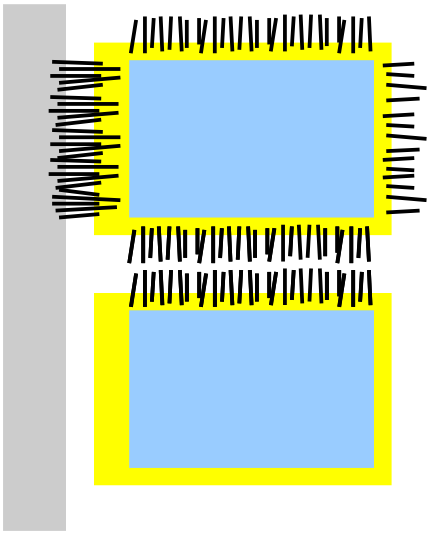


Option 2:

- 3x2 or 3x3 Mini@sics
- 102 – 121 channels
- channel pitch: 44um - 38um
- channel length: ~2.7mm or 4.4mm

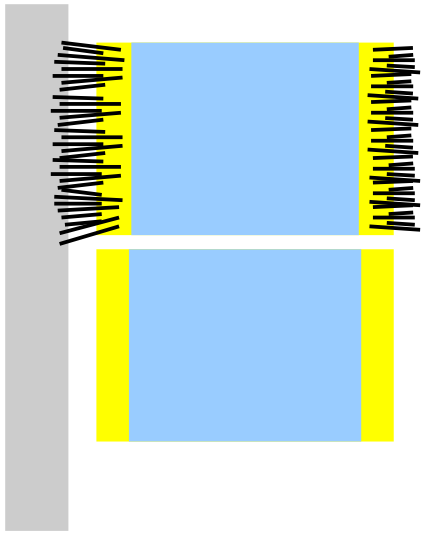
=> Poss. dimensions of UMC018 multi project waver runs are feasible in principle!

Basic Bonding Options



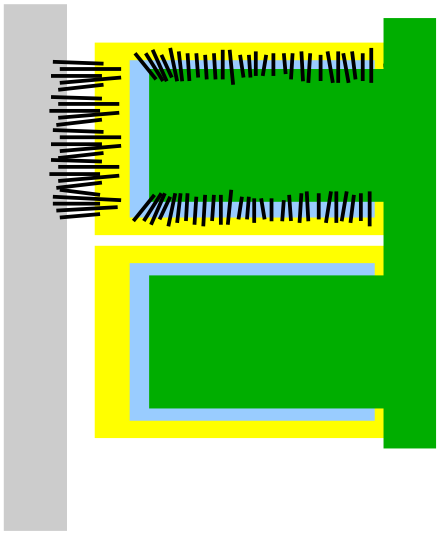
Option 1
Pad rows on sides

+ low voltage drop
+ many pins
- large gap
- bonding difficult



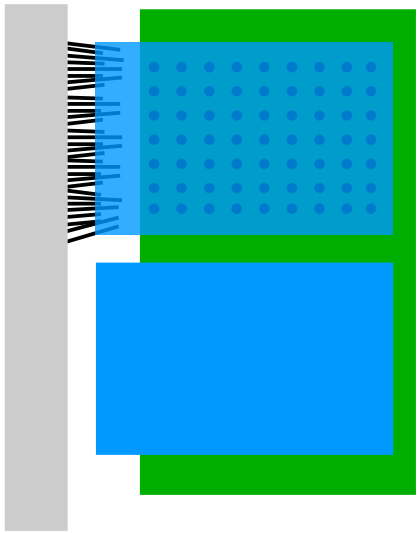
Option 2
No Pad rows on side

+ easy bonding
+ small gap
- high voltage drop
- pin limited



Option 3
Wire bonds to PCB

+ low voltage drop
+ small gap
- bonding tricky
- complex PCB

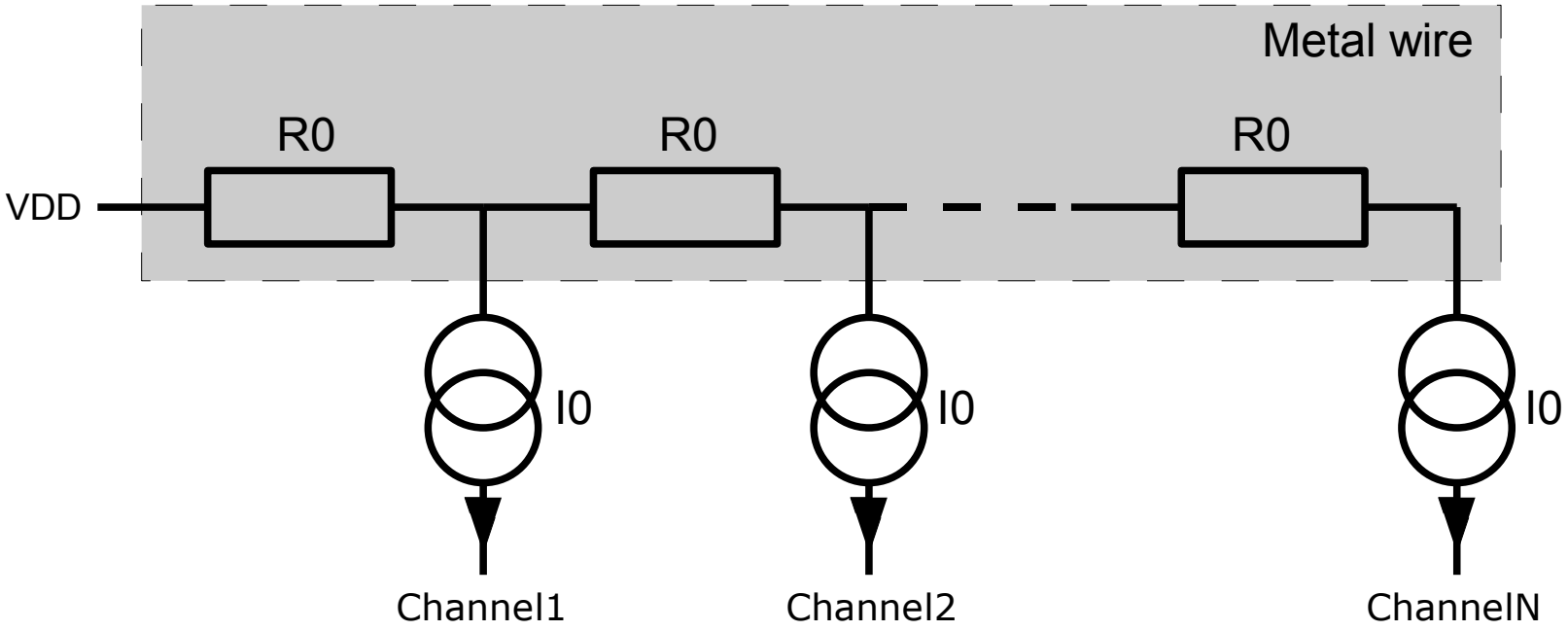


Option 4
Ball bonding to PCB

+ lowest voltage drop
+ small gap
+ no pin limitation
- two bonding techniques
- PCB difficult (bondable material)

Focus on Power Distribution (1)

- Simple model for calculating the voltage drop between channels:



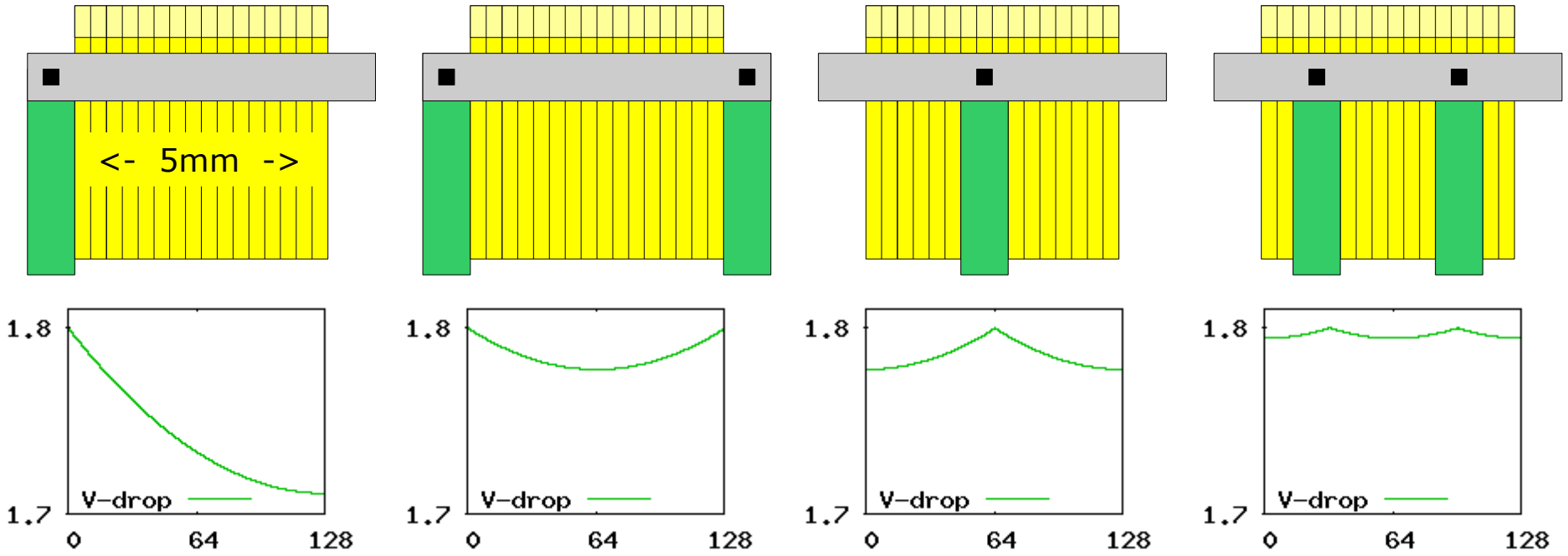
=> Voltage drop (n) = R0 * I0 * n (N - (n – 1)/2)

R0 is given by metal layer (30mΩ/sq for M6)
I0 depends on power consumption of a single channel

Focus on Power Distribution (2)

- Example: 1mm(!) Power wire to amplifiers (5mA / channel) @ 5mm chip with 128 channels

Analog Pads | Metal 6 wire
Channels | Metal 5 wire



max. V-drop: 89.7mV | max. V-drop: 22.7mV | max. V-drop: 22.7mV | max. V-drop: 5.9mV

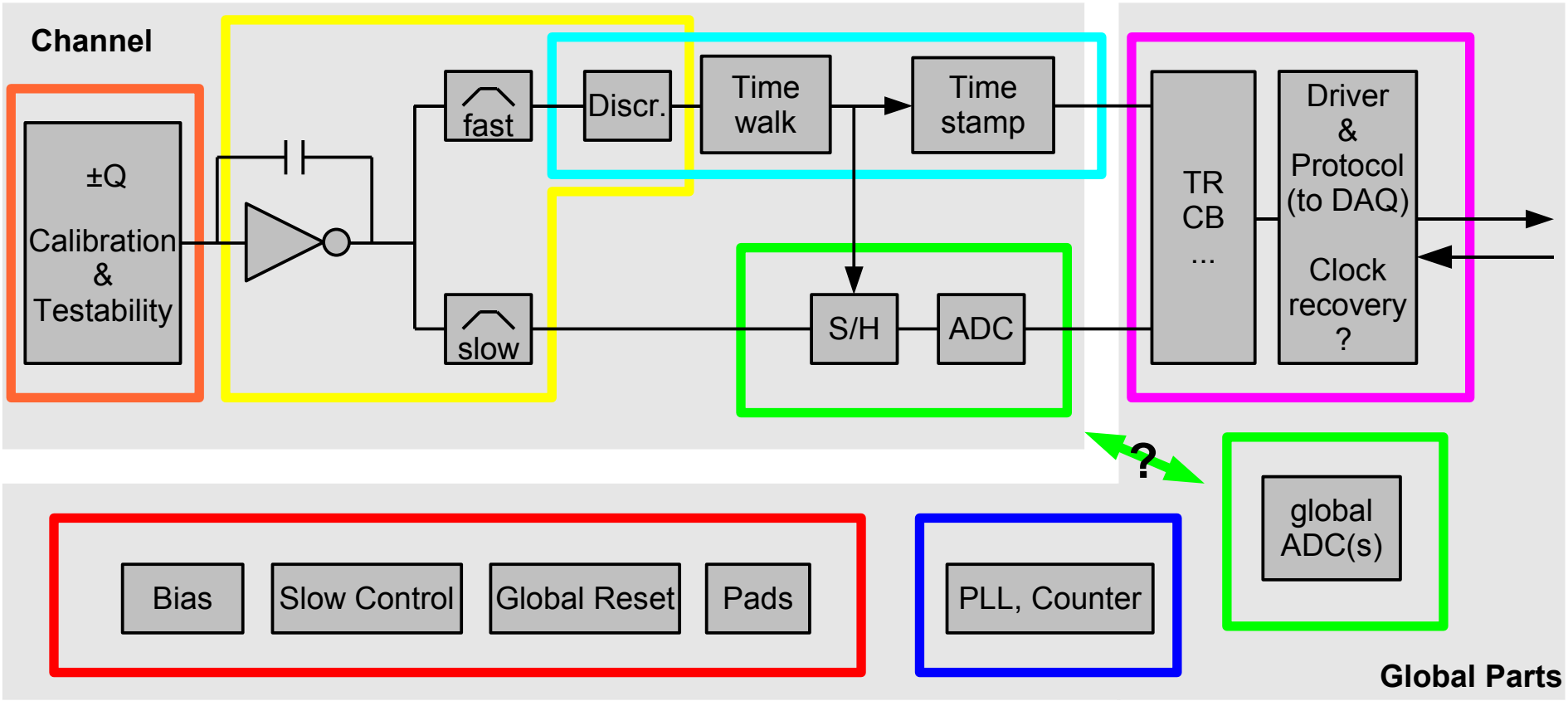
=> Voltage drop should be considered very early in design process.

Building Blocks

Architecture Based Working Packages

Good segmentation has to be found

- Cut where simple interfaces can be defined
- Some blocks can hardly be divided (e.g. preamp and shaper)
- Grouped blocks should be of one type (analog vs. digital, timing, amplifying, ...)



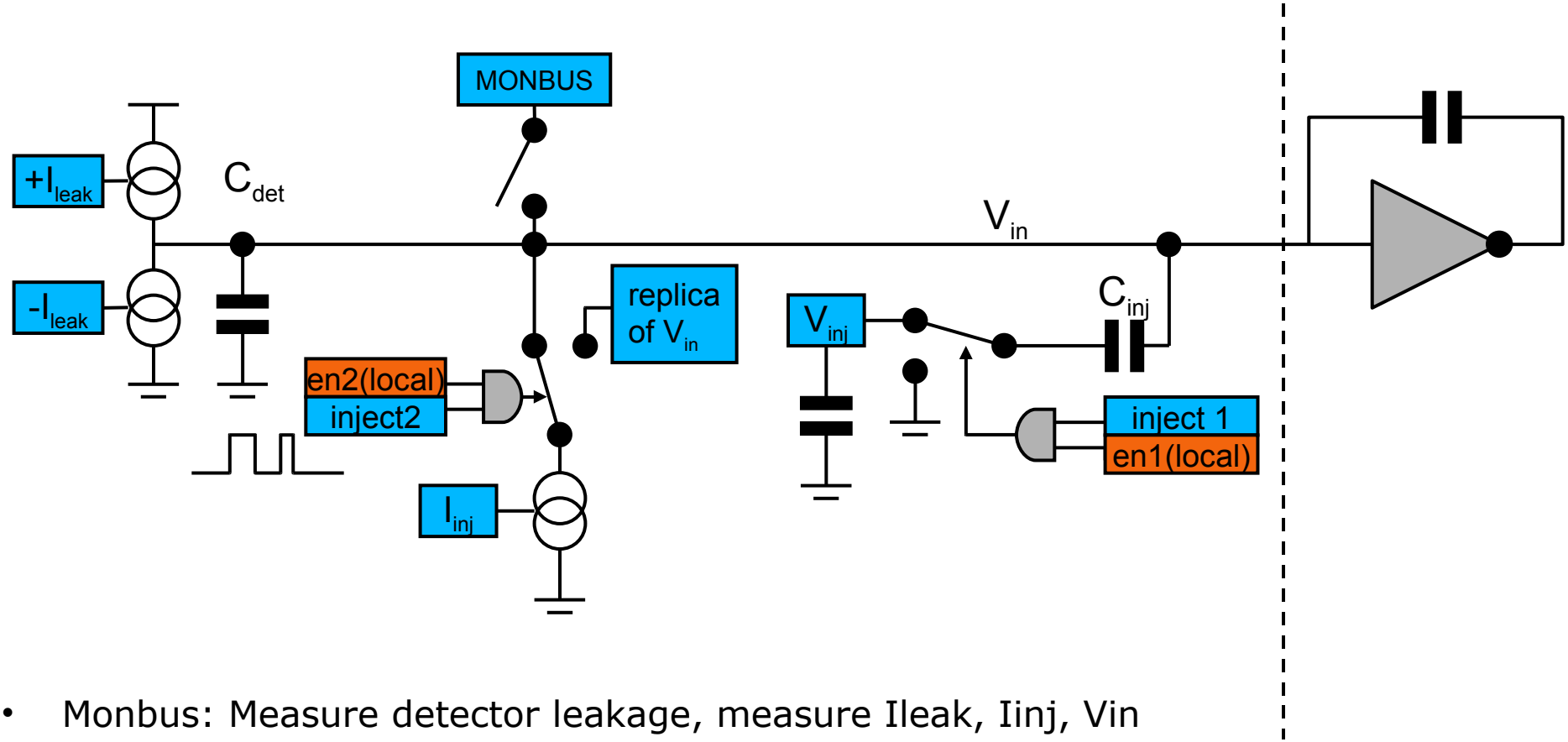
Working Packages in Detail

- Analog front-end (preamp, shaper)
  - Two shapers (fast and slow) seems to be a good choice
  - Think about differential signals (n-XYTER gets differential at slow shaper); simplifies polarity choice
- Injection circuit
  - Very important for calibration and testability, design carefully
- S/H and ADC
  - One ADC per channel or some ADCs per chip?
  - S/H could also be part of the TS/TW package (like n-XYTER)
- Discriminator, time walk, time stamp
  - TW is tricky, good idea is needed
- Tokenring or Crossbar, digital FIFOs
  - Complexity strongly depends on ADC decision
- Driver and protocol to DAQ
  - Good communication with DAQ people required
  - Event trigger strategy?
- PLL, global time stamp counter
  - Possible synchronizing strategies: Global reset via pin, use the DAQ I/O block, ...
- Bias, Slow control, Pads, ... (small peripheral parts)

Design carefully: Injection Circuit

- Goals:
  - Full chip characterization without external components
  - Measure Noise
    - fine steps up to ~ ½ mip
    - calibrated charge
    - Inject known step through known injection capacitor C_{inj}: $Q_{inj} = C_{inj} \times dV$
  - Measure dynamic range and (linearity)
    - larger steps up to ~ 4 mip
  - Measure timing and double pulse behavior
    - requires more than one step or – better – current pulses: $Q_{inj} = I_{inj} \times dT$
  - Measure tricky details
    - i.e. measure crosstalk: inject one channel, measure thres/noise on neighbor
  - Inject leakage current, measure leakage current
    - Versatile Monitoring Bus

Possible Circuit



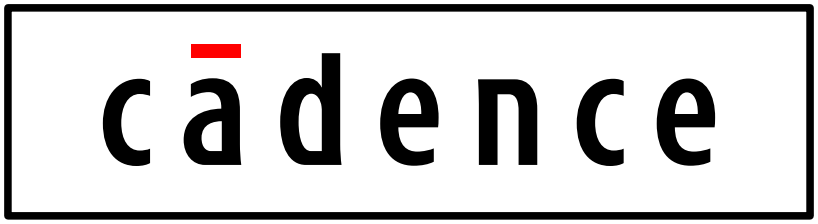
- Monbus: Measure detector leakage, measure Ileak, Iinj, Vin
- Add large array of Cinj with cap measurement on chip
- Cinj value: Cinj = Qmax / DVmax ~ 10fC / 1V ~ 10fF

Circuit to measure C_{inj} precisely

Cadence / File Organization

General Cadence Issues

- To avoid version complications minimum requirements have to be defined.
  - Cadence has migrated to open access (OA) database what implicit defines the minimal required version 6.0.
  - Data files generated with v.6.0 or higher should be compatible (no change in intern data structure).
  - Can L, XL or GXL (schematic, layout, ...) be mixed? Probably yes...? But some features of XL/GXL can't be used in L/XL.
  - Use same design kit version!
  - Note: If radhard layouts required, extraction files are available from Mannheim for assura. (Do we need some for calibre?)



- Next step: Collect what cadence versions are used by participating groups. Will everybody have access to OA soon?

Global vs. Local Libs

Designers hold their libs local

+ everybody is as free as possible in organizing his data / his files
+ fast access to lib(s)
+ general blocks still could be shared using a version control mechanism
- mediator needed (define and supervise interfaces)
- good and much communication needed (interfacing is error-prone)
- "synchronization" overhead is time-consuming
- bad surprises can occur if blocks are combined shortly before submission

Mount / synchronize / manage a global lib

+ work is intrinsically synchronized
+ everybody is up to date
+ designers can orientate on neighbor building blocks
+ global simulations *may* be possible early
- slow access to lib(s) (international team, high distances)
- data organization overhead (access control, fast server, ...)
- interfaces may "run out of control" => mediator still needed

Final Chip Assembly / Verification / Submission

- Global simulation / verification
  - Analog or mixed mode simulation of the hole chip is very complex or even impossible.
  - But: interfaces and timing needs to be checked.
  - Proposal: Every designer has to deliver (and hold up to date) a Verilog-A model of his building block(s). The mediator then is responsible for simulating the basic functionality of the hole chip while banking on given Verilog-A models.
- Proposal: “Semi”-Global Lib
  - Designers work local.
  - On fixed dates everybody delivers his files (only some needed views like schematics, verilog-a, layouts, ...) to a central lib.
  - Delivering could be done via copy script that makes a hierarchical copy of the top cells. Mannheim has already a skill based copy script that could be used as a starting point.
- Submission
  - Setting together building blocks and global DRS & LVS checks could be made by Mannheim

Summary

- Possible dimensions in UMC018 MPW runs are feasible for building the CBM-XYTER in principle. Up to 128 channels are realistic.
- We must decide on module mechanics soon.
- We must distribute building blocks soon. Mannheim volunteers for injection, global stuff and R/O interface.
- We should agree on Cadence & design kit versions.
- We must discuss and agree on library management approach.

Thank you!

Pinout and I/O Standards

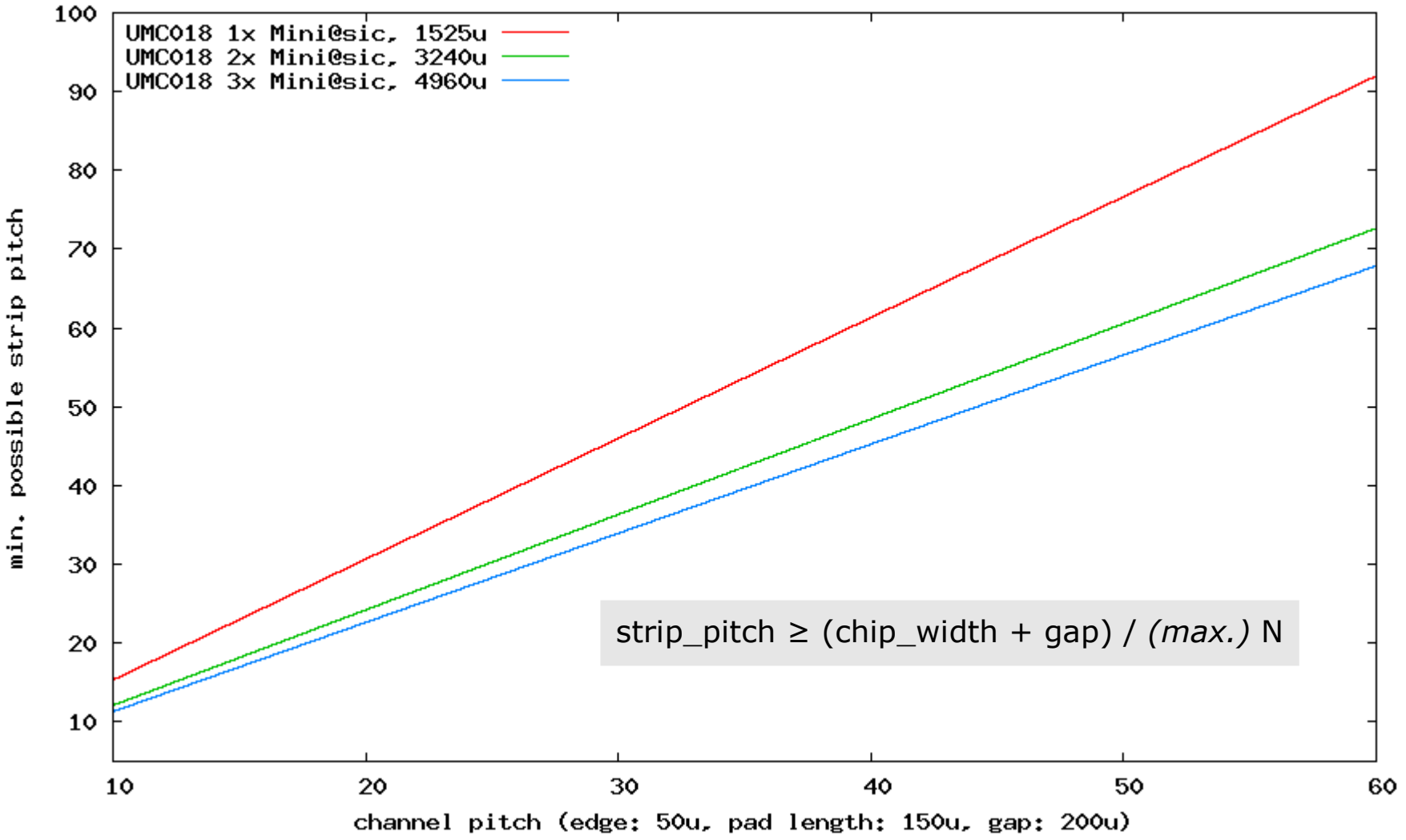
Pinout

- One analog input per channel
- Bias monitor/diagnostic pads
- Power nets
- Pad ESD protection
- I2C (Chip-ID, SCL, SDA, Reset, RegisterReset,
- Test I/O, Test-Trigger
- CLK inputs
- Resets
- LVDS (data, clock)

- See also n-XYTER...

Details über LVDS, Aussage???

Minimal Possible Stripe Pitch

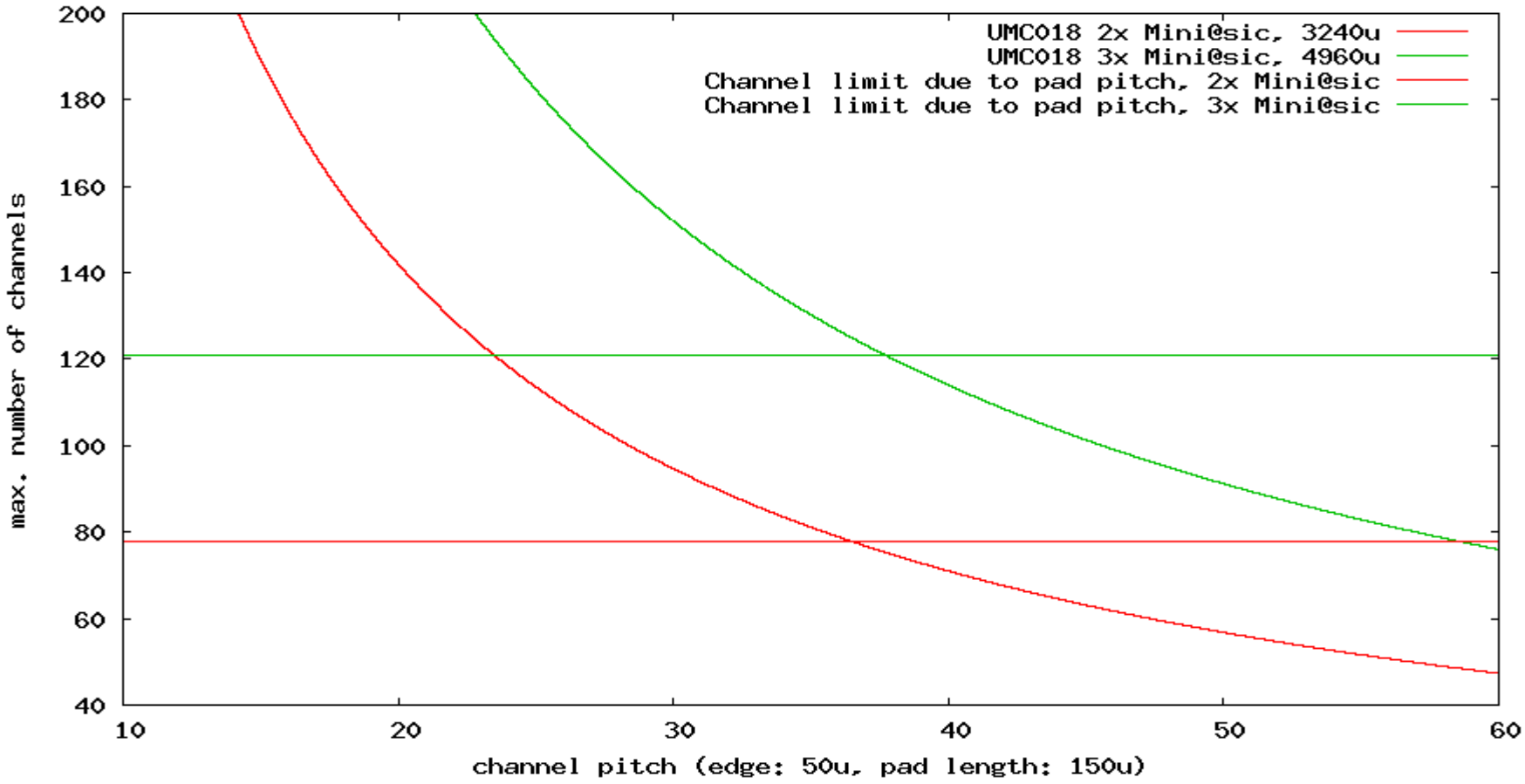


strip_pitch ≥ (chip_width + gap) / *(max.)* N

Maximal Number of Channels

chip_size = 2 * (pad_length + edge) + N * channel_pitch =>

(max.) N = (chip_size – 2*(pad_length + edge)) / channel_pitch



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  - Full 5 x 5 mm² runs every 2 month, 14.5k€
  - MiniASIC with blocks of (1.525mm)² every 4 months, 2.4k€ per block
  - ~2.5 months delivery
  - Cost break even at 6 MiniASIC Blocks !
- Scribe Line:
  - Taking the possible MiniASIC dimensions (see figure) the scribe line + seal ring seems to be <=190µm
  - Dicing is obviously done with a pitch of 1525µm + 190µm = 1715µm
  - We must therefore assume that the real chip size is (190µm – blade width) more than expected...
  - Note: In MPW chips may be larger due to cutting!